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An I-V Circuit with Combined Compensation for Infrared Receiver Chip

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Abstract – This paper proposes a novel combined compensation structure in the infrared receiver chip. For the infrared communication chip, the current-voltage (I-V) convert circuit is crucial and important. The circuit is composed by the transimpedance amplifier (TIA) and the combined compensation structures. The TIA converts the incited photons into photocurrent. In order to amplify the photocurrent and avoid the saturation, the TIA uses the combined compensation circuit. This novel compensation structure has the low frequency compensation and high frequency compensation circuit. The low frequency compensation circuit rejects the low frequency photocurrent in the ambient light preventing the saturation. The high frequency compensation circuit raises the high frequency input impedance preserving the sensitivity to the signal of interest. This circuit was implemented in a 0.6μm BiCMOS process. Simulation of the proposed circuit is carried out in the Cadence software, with the 3V power supply, it achieves a low frequency photocurrent rejection and the gain keeps 109dB ranging from 10nA to 300μA. The test result fits the simulation and all the results exploit the validity of the circuit.

Keywords: I-V converter, Photo current, TIA, Infrared receiver, Compensation structure

1. Introduction

Infrared (IR) communication technology uses the infrared light as the carrier to transmit the signal [1, 2]. The transmitter and the receiver use the modulation and coding technology to transfer the information. It has the advantage of low cost, stable performance and easy to implement. So it is widely used in the home appliances, remote control and infrared sensor, etc [3-5].

In general, the IR signal would be disturbed within the transmission channel. So the intensity of the signal becomes weak at the receiving port. Then the IR receiver chip is easily interrupted in the environmental light source, such as sunlight, the fluorescent and the incandescent lamp. This interrupt source produces the interference of the low frequency photocurrent (I_{ph}) [6, 7]. It will shift the DC working point and reduce the output swing even distortion at last. In order to improve the sensitivity for the infrared signal detection, how to suppress the interference in the low frequency I_{ph} with the ambient light effectively becomes a very important challenge. This paper proposes a novel combined compensation structure in the I-V conversion circuit which applied into the IR receiver chip. It restrains the low frequency I_{ph} noise effectively and improves the sensitivity of the IR receiver chip.

The IR communication has two parts: one is the transmitter and the other is the receiver. In this paper, the I-V convert circuit was designed in the receiver. The frequency range of the I_{ph} is 33 kHz~40 kHz. The functional block of the IR receiver is shown in Fig. 1.

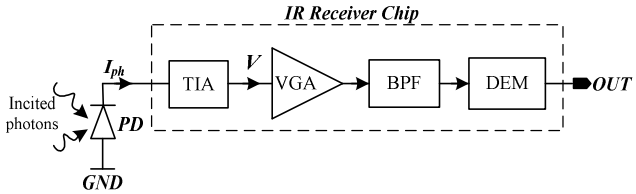

Fig. 1. Functional block of the IR receiver

In Fig. 1, when the transmitter sends out the infrared light, the photon reached the receiver in the air. When the photon incited the receiver, the photo detector (PD) converts the photon into I_{ph} [8, 9]. Because the I_{ph} is very weak, so the I-V converter amplifies I_{ph} and transforms it into voltage signal. The voltage is processed by the variable gain amplifier (VGA) and the band pass filter (BPF) [10, 11]. The VGA provides the gain of the system and the gain is adjusted according to the amplitude of the input signal. The BPF ensures the useful signal pass and block the signal out of its bandwidth. Then the signal passes through the demodulation (DEM) block to control the post-stage circuit.

2. Proposed I-V Converter

In fact, the scope of the I_{ph} from picoampere to hundreds microampere, the signal should be amplified to the post-stage circuit. So the gain of the TIA should be a few

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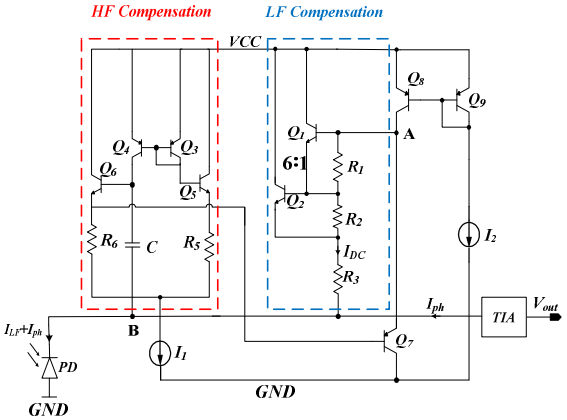

Fig. 2. Combined compensation I-V convert circuit

hundred thousand ohms at least [12, 13]. When the ambient light is stronger, the low frequency part in the I_{ph} would be hundreds of microampere. It could cause saturation of the receiver easily. To solve the problem, an improved variable resistance structure is used as the feedback gain [14, 15].

But with the equivalent resistor decreasing, the gain of the TIA will shutdown. Then the sensitivity of the circuit decreases. To solve the problem, we propose a novel I-V converter circuit which not only restrain the low frequency noise but also keep the gain of the TIA.

2.1 Combined compensation structure

To reject the frequency from DC current to the 30 KHz I_{ph} and keep the sensitivity of the receiver, the combined compensation structure is proposed [16]. It is showed in Fig. 2.

In Fig. 2, the blue block is the low frequency compensation circuit. It uses a variable resistance structure which equivalent resistance decreases with the input current increases [17]. The red block is the high frequency compensation circuit. It increases the resistance of the low frequency compensation circuit at signal frequency [18]. It could prevent the useful signal entering the low frequency compensation circuit. Consequently, the sensitivity will be improved significantly.

In Fig. 2, the LF pole point is in the HF compensation range. Because of the high capacitance of the pole, Q_6 is the pole point of the high frequency compensation. It was constructed by the capacitor C and the emitter small signal impedance of Q_6.

$$p_{1L} \approx \frac{1}{2\pi(C+C_{be})\cdot(R_6+\beta\cdot r_b)} \tag{1}$$

In (1), $\beta \approx \frac{\beta_0}{\sqrt{1+(f/f_\beta)^2}}$. β_0 is the intrinsic magnification and the $f_\beta \approx \frac{1}{2\pi(C_{be}+C_{bc})\cdot r_{be}}$.

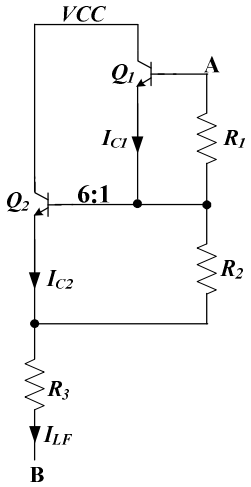

Fig. 3 Low frequency compensation circuit

The HF pole point locates in the LF compensation circuit. For the ratio of Q_2 to Q_1 is 6, the parasitic capacitance of Q_2 is large. Then the HF pole point is located here. The R_2+R_3 and the collector capacitance of the Q_2 constitute the HF pole point. It can be expressed:

$$p_{1H} \approx \frac{1}{2\pi(R_2+R_3)\cdot C_{Q_2}} \tag{2}$$

2.2 Low frequency compensation circuit

The low frequency compensation circuit uses the variable resistance structure [19]. It is showed in Fig. 3.

When R_1>>R_2>>R_3, the ratio of emitter area in Q_1 and Q_2 is 1 to 6. When I_{LF} is very weak, Q_1 and Q_2 turn off. The equivalent resistance of this circuit is:

$$R_{eq1} = \frac{V_{AB}}{I_{LF}} = R_1 + R_2 + R_3 \tag{3}$$

V_{AB} is the voltage between point A and B. With I_{LF} increases, Q_1 turns on and the equivalent resistance is:

$$R_{eq2} = \frac{V_{AB}}{I_{LF}} = R_1 + R_2 + R_3 - \frac{I_{C1}}{I_{LF}}R_1 \tag{4}$$

I_{C1} and I_{C2} are the current through Q_1 and Q_2, respectively. When I_{LF} becomes larger, Q_1 and Q_2 turn on and the equivalent resistance is:

$$R_{eq3} = \frac{V_{AB}}{I_{LF}} = (R_1 + R_2 + R_3) - \frac{I_{C1}+I_{C2}}{I_{LF}}R_1 - \frac{I_{C2}}{I_{LF}}R_2 \tag{5}$$

From Eq. (3)~(5), the equivalent resistance decreases with I_{LF} increases. That is to say, this circuit will separate the low frequency parts from the useful signal. So V_{out} would not saturate even the larger I_{LF} entering the receiver.

2.3 High frequency compensation circuit

But the low impedance circuit would shunt parts of the I_{ph}. It would cause a voltage drop ΔV_B at point B. So, in Fig. 2, this paper constructed the high frequency compensation circuit with the capacitor C between the input and the Q_6. Through the C, Q_6 and Q_7, the similar voltage drop ΔV_A at point A.

Q_3 and Q_4 is the current mirror with the ratio of 1:1. Q_5, R_5, Q_6 and R_6 construct the symmetrical structure. So the base voltage of Q_6 is:

$$V_{BQ_6} = V_A = VCC - V_{BE} \tag{6}$$

V_{BE}: emitter-base voltage. In the photovoltaic mode, the PD works in the reverse biased voltage, the biased voltage reducing the parasitic capacitance and increasing the drift speed in the depletion layer. It could improve the response time of the PD. Using the R_1~R_3 as the bleeder resistor, so the reference voltage of the PD is:

$$V_B = V_A - (V_{R1} + V_{R2} + V_{R3}) \tag{7}$$

From Eq (6), with the increase of I_{ph}, the reference voltage of the PD would decrease. For the I_{ph}, the impedance of the low frequency compensation is so large, and then majority I_{ph} flows into the TIA module. So the sensitivity of the receiver will not decline sharply when there the large I_{LF} occurs.

2.4 TIA circuit design

TIA converts I_{ph} into voltage signal. In order to amplify the input signal and not lead to the output saturation [20]. The TIA used two negative feedback loops. The circuit showed in Fig. 4.

In Fig. 4, because of the current I_{ph} may be mixed with the low frequency components, the capacitor C_{TIA} could insulate the low frequency components in the I_{ph}. R_7 is the current limiting resistor. R_7 and Q_1~Q_5 construct the DC negative feedback loop. The inverting input voltage is $V_-=V_+=V_{ref1}$. R_f is the AC negative feedback resistor. When the V_- becomes higher, the V_{out} decrease too. Then the current I_1 and I_2 drop down, it induces the current flow through Q_4 and Q_5 becomes lower. Then the voltage V_- drops down.

Here the amplifier in Fig.4 can be equivalent to a single pole system which gain is G and the single pole is $-1/a$.

Because I_{ph} is very weak, in order to reduce the saturation of the output, the R_f should exceed R_1+R_2+R_3 in Fig. 2. It could improve the DC impedance and prevent the saturation distortion of the output.

Combined the Fig. 2 and Fig. 4, the equivalent model of the optoelectronic process circuit can be showed in Fig. 5. The R_p is the equivalent resistor from the point B except the TIA circuit in Fig. 2. The C_{TIA} is the equivalent capacitor and the R_{feq} indicates the equivalent resistor except the C_{TIA} in Fig. 4. The I_{Rf} is the current flow through feedback resistor R_f in Fig. 4.

The R_p can be calculated from Fig.2 which is given by Eq. (8):

$$R_p = (R_1 + R_2 + R_3) \cdot (1 + sr_cC) = R_{p0}(1 + sr_cC) \tag{8}$$

Where, r_c is the equivalent resistor of Q_4 collector and C is the capacitor in Fig. 2. From Fig. 4, R_{feq} can be expressed by Eq. (9):

$$R_{feq} = R_f \frac{1 + sa}{G + 1 + sa} \approx \frac{R_f}{G + 1} \tag{9}$$

Where, G is the amplifier gain in Fig. 4. From Fig. 5, I_{Rf} is obtained:

$$I_{R_f} = I_{ph} \frac{\frac{1}{R_{feq}}}{\frac{1}{R_{feq}} + sC_{TIA} + \frac{1}{R_p}} \tag{10}$$

Substitution of Eq. (8) and Eq. (9) into Eq. (10) yields:

$$I_{R_f} = I_{ph} \frac{R_{p0}(1 + sr_cC) \cdot (G + 1)}{(G + 1)R_{p0}(1 + sr_cC) + sC_{TIA}R_fR_{p0}(1 + sr_cC) + R_f} \tag{11}$$

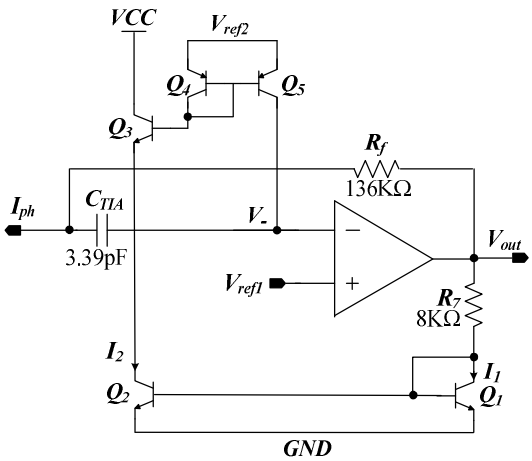

Fig. 4. TIA circuit

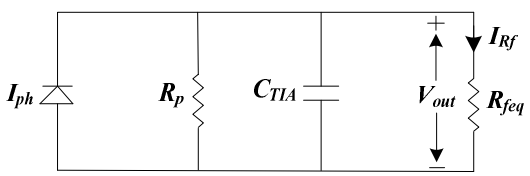

Fig. 5. Equivalent optoelectronic process circuit

Then the output voltage V_{out} can be showed:

$$V_{out} = I_{R_f} \cdot R_{feq} \tag{12}$$

So when the frequency is lower, the transfer function can be showed:

$$H(s) = \frac{V_{\text{out}}}{I_{ph}} = \frac{R_{p0}(1+sr_cC)\cdot(G+1)}{(G+1)R_{p0}(1+sr_cC)+R_f} R_{feq} = \frac{R_{p0}(1+sr_cC)\cdot R_f}{(G+1)R_{p0}(1+sr_cC)+R_f} \tag{13}$$

With the increasing of the frequency, the V_{out} becomes higher but when the frequency becomes very high, for the influence of s^2 item in the C_{TIA}, the V_{out} will become lower.

3. Result and discussion

The IR receiver chip is fabricated by the 0.6μm BiCMOS process. Its area is 1.2*1.2 mm^2. The photograph is shown in Fig. 6.

3.1 Simulation result

In order to test the compensation effect of the combined compensation structure, this paper used the 0.6μm BiCMOS process and simulated the proposed circuit with the Hspice software. When the temperature is 25℃and the VCC=3V, simulates the single compensation and the combined compensation circuit, respectively. When the LF signal varied from 10 nA~300 μA, the single compensation circuit without the HF compensation was simulated and the result is shown in Fig. 7.

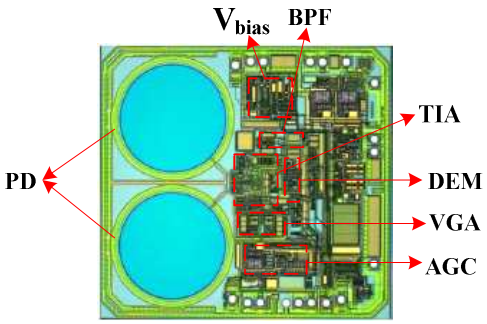

Fig. 6. The chip photograph

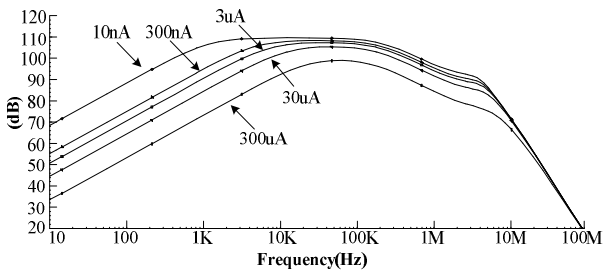

Fig. 7. Frequency response of the single compensation

The transimpedance gain without high frequency compensation circuit changed very large from 10nA to 300μA. The gain declined from 109dB to 90dB sharply. With the declined of the gain, the sensitivity of the receiver reduces. When the TIA circuit uses the high frequency compensation structure; the gain can be controlled by the double compensation structure. The frequency response with the double compensation are illustrated in Fig. 8.

With the low frequency signal varied from 10nA~300μA, the transimpedance gain of the I-V converter keep the same value 109dB. It ensures the sensitivity of the PD for the different input optical signal.

3.2 Test result

To compare the bit error rate of the combined compensation and the single compensation, we use the Agilent N9320B to show the eye diagram. The 9 Kbps ~ 28Mbps BMC (Biphase Mark Code) random pattern data are used in the input port. The random input data is simulated by the BMC, so 25Mbps = 40UI (Unit Interval). Then the 192 KHz input signal can be generated. If the chip can work well with the 192 KHz signal, it must be better with the 33 KHz~40 KHz input signal. In order to achieve the high speed communication signal integrity, here we choose the 25Mbps data as the input data then the

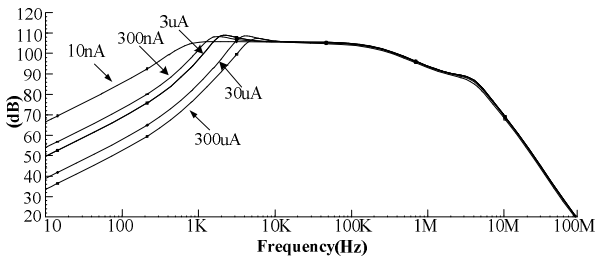

Fig. 8. Frequency response of the double compensation

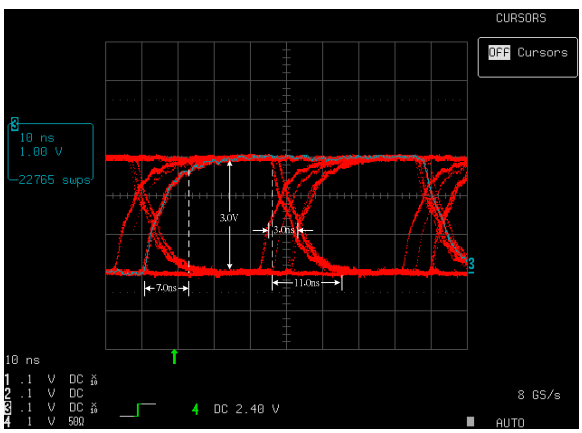

Fig. 9. The eye-diagram in the single compensation circuit

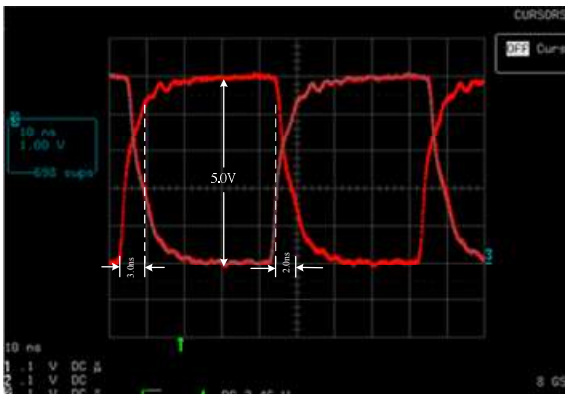

Fig. 10. The eye-diagram in the combined compensation circuit

Talbe 1. Parameter comparison of the eye-diagram

Parameter Name	Parameter value	
	Single compensation	Combined compensation
Height	3.0V	5.0V
Rise time	7ns	3ns
Fall time	11ns	2ns
Peak-peak jitter	3ns	<1ns

eye diagram is generated, which works at temperature 25℃ with VCC=3V.

Fig. 9 shows the eye-diagram in the single compensation circuit. The jitter and distortion occur in the area of the crossing. The height of the eye-diagram is 3.0V. The rise time is 7ns and the fall time expanded to 11ns. When the 1UI = 1/25Mbps = 40 ns, the jitter could reach 3.0ns. It indicates that the bit error rate increased in the single compensation circuit sharply.

Fig. 10 shows the eye-diagram in the combined compensation circuit, from which it can be seen that the height expands to 5.0V. The rise time is 3ns and the fall time is 2ns. The jitter in the area of the crossing disappears. It indicates the bit error rate is reduced sharply. The larger the amplitude of the eye-diagram, the better the effect of the communication is. Thus, the advantages of the combined compensation circuit can be seen from the amplitude value for the different amplitude of the experiment results. It is testified that the combined compensation structure rejects the interrupt in the I_{ph} and suitable for the IR receiver chip. The key parameter was compared in Table 1.

4. Conclusion

The I-V converter with the combined compensation is investigated in 0.6μm BiCMOS process. It rejects the low frequency input current and keeps the high sensitivity of the receiver. The results have showed that the circuit provides a transimpedance gain of 109dB and can reject the low frequency currents from 10nA to 300μA.

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