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FPGA Implementation of Diode Clamped Multilevel Inverter for Speed Control of Induction Motor

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Abstract – This work proposes FPGA implementation of Carrier Disposition PWM for closed loop seven level diode clamped multilevel inverter in speed control of induction motor. VLSI architecture for carrier Disposition have been introduced through which PWM signals are fed to the neutral point seven level diode clamped multilevel using which the speed of the induction motor is controlled. This proposed VLSI architecture makes the power circuit to work better with reduced stresses across the switches and a very low voltage and current total harmonic distortion (THD). The output voltages, currents, torque & speed characteristics for seven level neutral point diode clamped multilevel inverter for AC drive was studied. It has observed the proposed scheme introduces less distortion and harmonics. The results were validated using real time results.

Keywords: VLSI Architecture for PD carrier PWM, FPGA, Diode clamped MLI, Total Harmonic distortion

1. Introduction

Over the years [2] the requirement of high power instruments is a need in industrial applications. A Multilevel power converter acted as a replacement in high and medium voltage requirements in industries. The basic idea behind these multilevel inverters is to use a set of semiconductor switches that is connected to different low voltage DC sources which in turn produce staircase voltage capable of producing high power. The balancing of voltage is a problem with DC capacitors in all multilevel inverter with multiple DC links. The author [3] proposes a chopper based solution to eliminate the unbalance of the voltage that occurs in capacitors. [1] This work uses carrier based space vector pulse width modulation Technique to drive the IGBT's used in a Three Level Diode Clamped multilevel inverter for PMSM drive. The performance of the system was studied using the speed characteristics, torque, output voltage and current. Multilevel inverters are capable of operating at high switching frequencies and capable of producing a low level harmonics [4-9]. Multilevel converters generate a lower common mode voltage. Hence the bearing of the motor attains s lower stress when connected to multilevel motor drive. These common mode voltages can be removed using different modulation schemes [10]. Several Carrier based PWM techniques had been formulated for controlling the active devices in a multilevel inverter. In general there are three carrier based techniques that are used in multilevel inverters: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). For Industrial applications SPWM is most often used. In order to enhance the DC link utilization third harmonic injection PWM is used [11].

Over the yester years many researchers have developed 3 level, five level diode clamped multilevel inverter was developed with different PWM technique and the same PWM technique was implemented using microcontrollers or DSP controllers. In multilevel inverter, a general compromise should arrive between the large number of switches for large number of levels and reduce the THD. Significant reduction in THD is usually achieved in seven level multilevel inverter. Increasing the levels beyond seven may leads to higher complex circuit and higher cost, but with a small reduction in THD[12]. In Induction motor reduction of 3^{rd}, 5^{th} and 7^{th} harmonics are significant requirement than THD and so seven level is sufficient, which reduces these significant harmonics to lower level. [13]

In seven level diode clamped multilevel inverter share a common dc bus for all the three phases, which leads to implementation of back to back converter motor for motor speed control applications. Very few researches had attempted to implement the PWM technique on the FPGA. This work implements the PD PWM technique on a FPGA, which is used for controlling the speed of induction motor.

Section 2 gives the working of the three phase seven level diode clamped multilevel inverter. Section 3 & 4 Non-shoot through and shoot through modes. Section 5 illustrates the different PWM techniques used for simulation of the proposed power circuit. Section 6 gives the simulation and discussions of the power circuit fed on induction motor with different PWM techniques. Section 7 gives the FPGA implementation of Phase disposition PWM

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technique. Sections 8 discuss the hardware of the proposed methodology. Section 9 gives the conclusion.

2. Three Phase Seven Level Diode Clamped Inverter

A diode clamped multilevel as shown in Fig. 1 (K levels) inverter holds (K-1) capacitors in the DC bus and capable of producing K level on the phase voltage. The figure shows the one leg of seven level diode clamped multilevel inverter. The Dc bus has six capacitors (c1-c6) and switches are numbered as S1 – S12. Also the Z source network is the combination of L-C and the voltage across each capacitor through the clamping diodes is given as Vdc /2, Vdc/3 & Vdc/6, 0 –Vdc/2, -Vdc/3 & -Vdc/6 respectively. Hence an m level inverter leg has (K-1) capacitors and 2(K-1) switching devices and (K-1) (K-2) clamping diodes. One leg of seven level inverter is considered for the production of output staircase voltage. Each single phase bridge has two legs and the DC rail acts as the reference point for the output phase voltage. The following are the different seven level output voltage.

1. The upper half switches of S1 through S6 are turned on for the output voltage level of Vao = Vdc/2.
2. The upper five switches of S2 through S6 and one lower switch S8 are turned on for the output voltage level of Vao = Vdc/3.
3. The four upper switches of S3 through S6 and two lower switch S7 & S8 are turned on for the output voltage level of Vao = Vdc/6.
4. The three upper switches of S4 through S6 and three lower switch S7 – S9 are turned on for the output voltage level of Vao = 0.
5. The two upper switches of S5 through S6 and four lower switch S7 –S10 are turned on for the output voltage level of Vao = -Vdc/6.
6. The upper switches S6 and five lower switch S7 – S11 are turned on for the output voltage level of Vao=-Vdc/3.
7. The switch S7 – S12 are turned on for the output voltage level of Vao = -Vdc/2.

The Table 1 illustrates the different voltage levels and their individual switching states. The condition for switch is on indicate state 1 and switch 0 for off condition of the switch. Each switch is turned only once in each cycle and has six switches that are complementary pairs in each of the phase. The pair of switches in each leg of the inverter (S1, S7), (S2, S8), (S3, S9), (S4, S10), (S5.S11), (S6, S12). Thus the switches are mutually exclusive. At a time six switches are switched on. One half of the sine wave is tracked by each of the phase leg voltage. The positive phase leg voltage of terminal a and the negative phase leg voltage of terminal b constitutes the line voltage. The line voltage results in stair case wave. This indicates that for a K level output phase voltage and (2K-1) level output line

Table 1. Switch states for three phase seven level diode clamped inverter

SWITCH STATES												O/P
S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	(Van)
1	1	1	1	1	1	0	0	0	0	0	0	Vdc/2
0	1	1	1	1	1	0	1	0	0	0	0	Vdc/3
0	0	1	1	1	1	1	1	0	0	0	0	Vdc/6
0	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	- Vdc/6
0	0	0	0	0	1	1	1	1	1	1	0	-Vdc/3
0	0	0	0	0	0	1	1	1	1	1	0	-Vdc/2

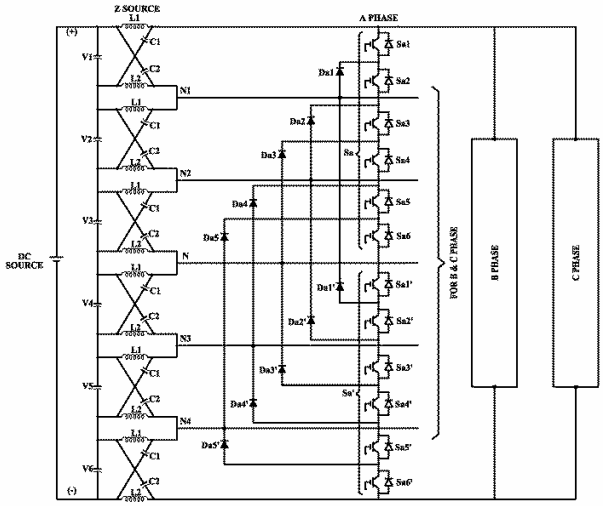


Fig. 1. Three phase seven level diode clamped inverter

voltage are obtained for a K level converter. Fig. 1 illustrates the power circuit of three phase Z source seven level neutral point diode clamped multilevel inverter. The proposed power circuit operates in two modes. 1. Shoot through mode and 2. Non-shoot through mode.

3. MODE 1- Non shoot through mode

The equivalent circuit during non shoot through mode is shown in Fig. 2. A The inverter is in a non shoot-through state that is one of the six active states and two traditional open zero states and inductor current meets the following inequality:

$$i_L > 0.5\ I_i \quad (1)$$

In this mode, the input DC current is

$$Iin = IL1+IC1 = IL1+(IL1-i1) = 2iL - i1> \quad (2)$$

Voltage across the inductor is

$$VL = V0-VC \quad (3)$$

Where $\mathbf{V_0}$ is the source voltage and Inductor current linearly decreases.

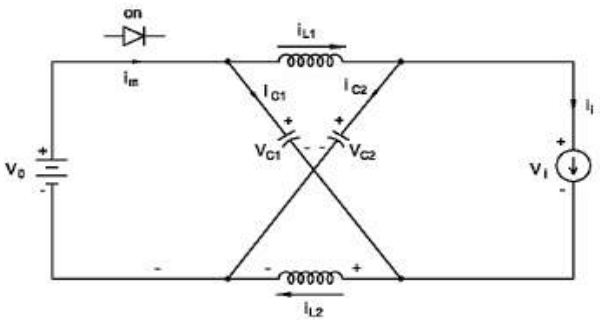


Fig. 2. Non shoot through mode equivalent circuit

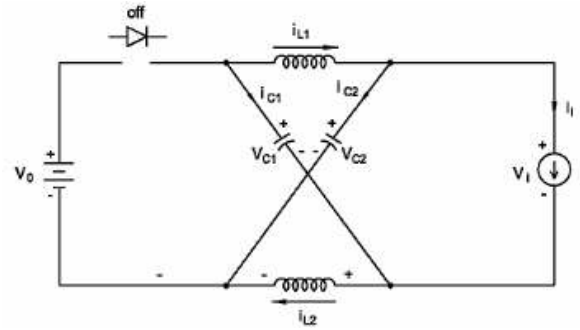


Fig. 3. Shoot through mode equivalent circuit

4. MODE 2- Shoot through mode

The equivalent circuit in shoot through mode is shown in Fig. 3. A switch shoot-through zero state occurs when the switches in any of the three phase legs are gated simultaneously. This mode produces a zero voltage vector at the inverter output like open mode and contributes to the total active length of zero voltage state.

In this mode VC1 + VC2> V0 (4)

The diode is reverse biased, and the capacitors charge the inductors.

The Voltages across the inductors are:

VL1 = VC1 and VL2 =VC2 (5)

The inductor current linearly increases.

5. PWM Techniques

Over the yester years various PWM techniques were used for multi level inverters. The renowned PWM methods used for multi-level inverters are the carrier based PWM (SPWM) techniques and the space vector based PWM (SVPWM) techniques. The SPWM schemes are easy to implement and more flexible. These SPWM techniques use a triangular carrier waveform as carrier and sinusoidal signal as reference signal. Multilevel sinusoidal PWM

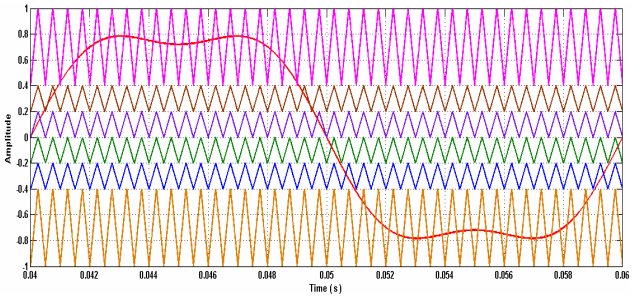


Fig. 4. Phase disposition PWM

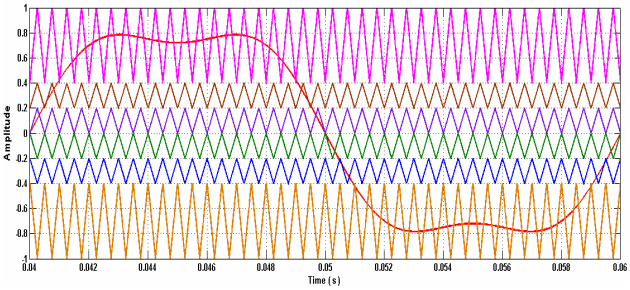


Fig. 5. Phase opposite disposition PWM

are further classified into carrier and modulating signals. Based on the carrier signals the technique is further classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique.

5.1 Phase disposition PWM technique

In this method all the carriers have the same frequency and amplitude. Also, the N-1 carriers are in phase with each other. This method uses N–1 carrier signals to generate N level inverter output voltage. All the carrier signals have the same amplitude, same frequency and are in phase [14]. Fourteen triangular carrier wave form is compared with one sine wave. Fig. 4 illustrates the PDPWM technique.

5.2 Phase opposite disposition PWM

In this technique, the carrier signals about the zero reference has same frequency, amplitude and in phase to each other [14]. But below the zero axis the carrier signals are phase shifted by 180 degrees. It requires m-1 triangular carrier signals and the reference is sinusoidal in nature.

The important harmonics is centered at F_c and other frequency appear as side bands around F_c. The technique is illustrated in Fig. 5.

5.3 Phase shifted carrier control technique (PS)

In this technique the carrier signals are 90 degrees phase shifted to each other. All the triangular carrier have the same frequency and peak to peak amplitude. For an m

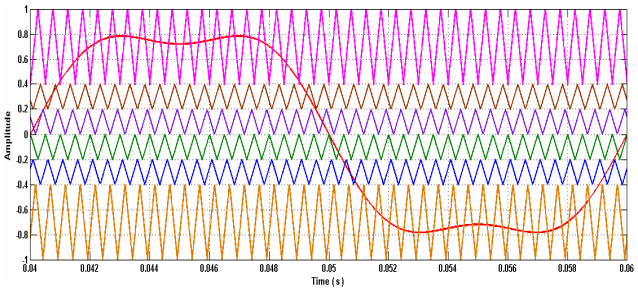


Fig. 6. Phase shifted carrier control technique

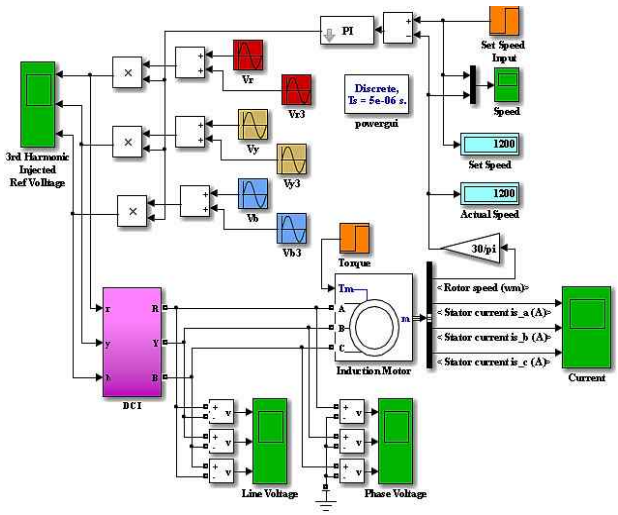


Fig. 7. Simulation of seven level diode clamped multilevel inverter

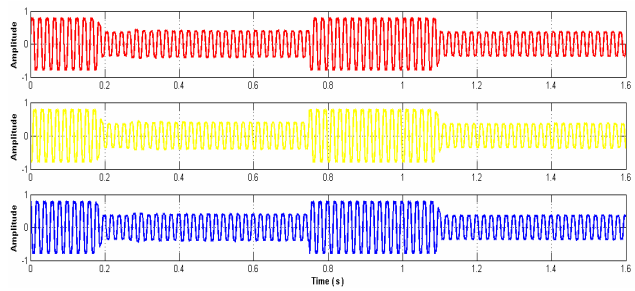


Fig. 8. Third harmonic injected reference waveform

voltage level required, m-1 carrier signals are required and they are shifted in phase by an angle θ=(360°/m-1). Fig. 6 illustrates the Phase shifted carrier control technique [15].

5.4 Simulation results and discussions

The Proposed power circuit, was three phase seven level neutral point clamped inverter fed Ac drive was simulated for three different PWM techniques such as PD,POD and PS. The quantitative parameters such as phase voltage THD, line voltage THD, Stator current THD, settling time and Stress across switches were compared based on the PWM technique applied to the power circuit. The entire

Table 2. Comparison of different measures on various PWM techniques on seven level diode clamped multilevel inverter

PWM	PH(V) THD	L(V) THD	STA(I) THD	(V) STR	SPD SET (t)
PD	29.98%	12.98%	1.55%	50V	0.2sec
POD	20.11%	20.38%	2.93%	50V	0.25 sec
PS	85%	74.98%	9.98%	50V	0.29 sec

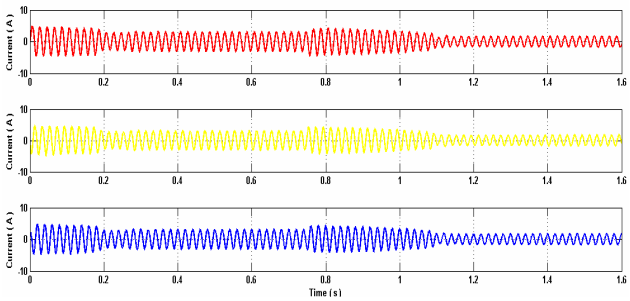


Fig. 9. Stator current for phase disposition carrier PWM

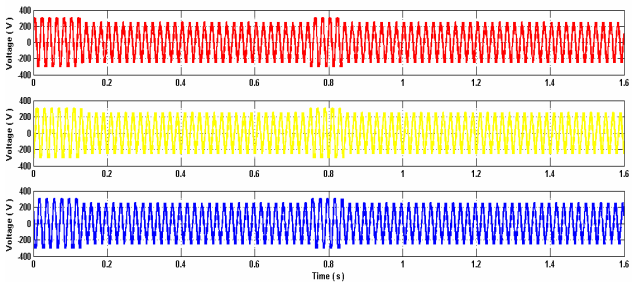


Fig. 10. Line to line voltage for in phase disposition carrier PWM

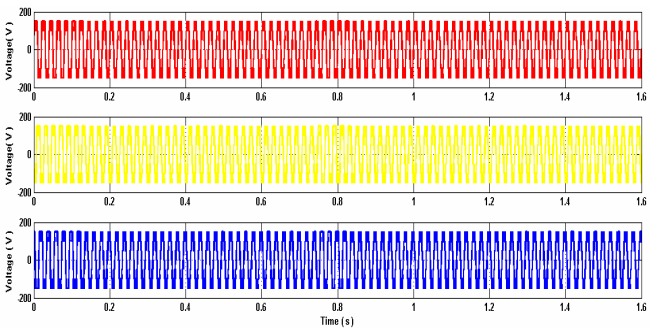


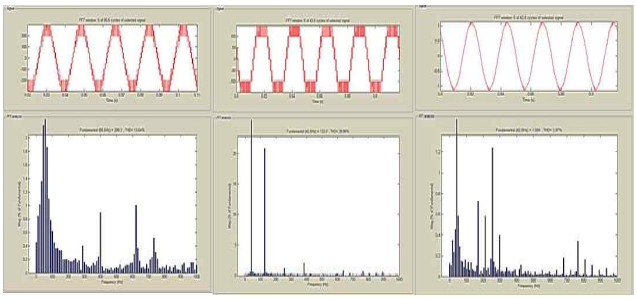
Fig. 11. Phase voltage for phase disposition carrier PWM

simulation was done in MATLAB and the results are shown:

Table 2 gives the quantitative measures of different PWM techniques on seven level diode clamped multilevel inverter. Fig. 7 illustrates the simulation of seven level diode clamped multilevel inverter. Fig. 8 gives the third harmonic injected reference waveform. Fig. 9 to 11 illustrates the Stator Current, Line to Line Voltage & Phase Voltage for Phase Disposition Carrier PWM. Fig. 12 gives the line to line voltage, phase voltage and stator current

Table 3. Parameters used of power circuit used for simulation

DC Link (V)	300 V DC
Inverter power (W)	200 Watts
Inverter O/P (V)	0-200 V AC Rms (Line to Line)
Switching freq.	2000 Hz
No. of carrier	6 Nos.



(a) (b) (c)

Fig. 12. Various THD measured during simulation for PD PWM technique. (a) Line to line voltage THD (b) Phase voltage THD (c) Stator current THD

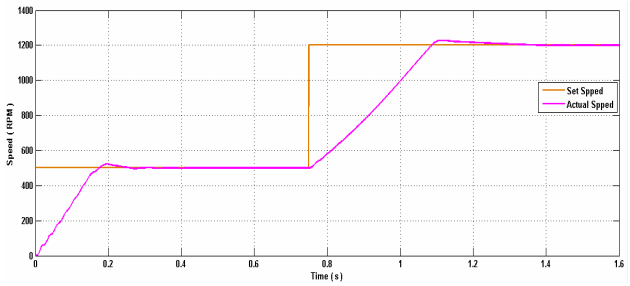


Fig. 13. Reference and actual speed

THD measured during simulation for PD PWM technique. Table 3 gives the design parameters used for simulation. Fig. 13 gives reference and actual speed of induction motor. The closed loop constants are obtained from Zeiger Nichols method.

7. FPGA Implementation of Phase Disposition PWM

From the above simulations it was observed that the PD PWM technique was found to give a reduced THD. So for high speed implementations FPGA was considered. A novel sequential architecture for PDPWM was implemented in the targeted FPGA as shown in Fig. 14.

The simulation was done using Model sim 5.8i and synthesis was done using XST of Xilinx project manager. The code was targeted to XC6SCX25-3ftg256 FPGA. The sequential architecture for the Phase disposition PWM is given below. The architecture is made of 1.

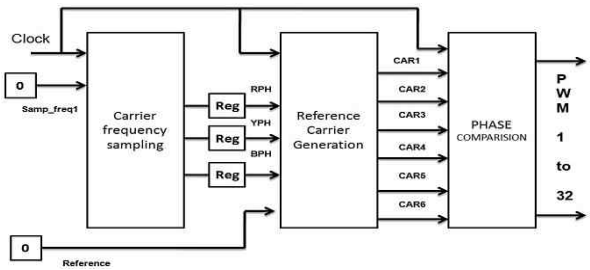


Fig. 14. Proposed Sequential Architecture for PDPWM

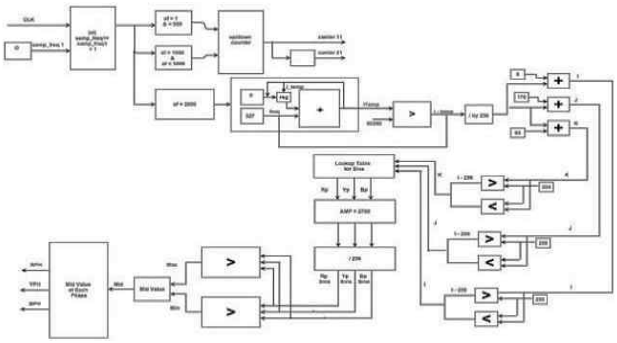


Fig. 15. FPGA architecture for Carrier frequency sampling module

Carrier frequency sampling 2. Reference carrier generation 3. Phase comparison.

7.1 Carrier frequency sampling module

Based on the rising edge of the clock the sine signal is sampled at 10 KHz. Once in every 10 KHz the frequency is incremented. When the maximum frequency is reached then the incremental steps is initialized into initial condition. For every 10 KHz once the value will be updated to the maximum count value and hence the signal will look like a ramp signal. Fig. 15 illustrates the FPGA architecture for Carrier frequency sampling module as shown.

7.2 Reference carrier generation module

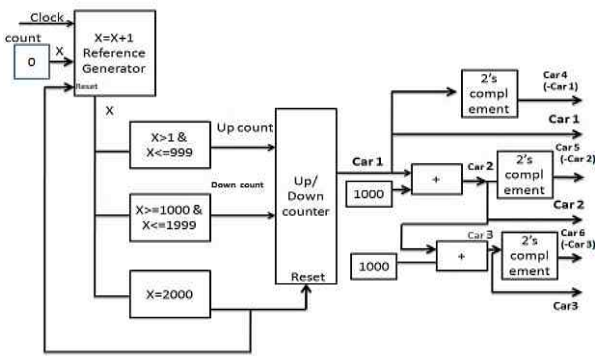


Fig. 16. FPGA architecture for Reference carrier generation module

7.3 Index calculation:

Index value for the sine signal stored in the form of look up table is generated here. For every clock cycle the index value increments by 1. The maximum 8 but value is 360 for 1 degree it is 0.71. Hence for R phase the 0.71 is multiplied by 0.71, B phase the 0.71 is multiplied by 240 and for Y phase 0.71 is multiplied by 120. Thus the index values for different phase are calculated. Also check the index value exceeds the maximum values; otherwise keep the computed index value for all the three phase. . Now calculate the corresponding sine values from the look up table using the precomputed index values. From the computed values find the Maximum, minimum and the middle value from the pre computed sine value. Based on the above pre computation the respective phase is added with middle value to give the corresponding phase values.

7.4 Reference sampling

The 10 KHz signal is chosen and if the reference signal is below 5 KHz then carrier 1 is incremented by 1. If the reference signal is between 5 KHz and 10 KHz then the carrier 1 is decremented by 1. If the reference signal is above 10 KHz then the carrier 1 gets reset.

Based on the carrier 1 other carriers are generated as shown in Fig. 15.

Carrier 2= carrier1 +1000
Carrier 3= carrier2+1000
Carrier4= - carrier 1
Carrier5= - carrier2
Carrier 6= - carrier3

7.5 Phase comparison module: R phase, Y phase, B phase

If the generated carrier is less than the reference sinusoidal signal then the generated PWM signal will be high otherwise the signal will be low. If the (carrier3 -60) is less than the sinusoidal extracted from the look up table then PWM output will be low otherwise the output will be high. From 6 carriers we generate 12 PWM signals. Similarly for other two phases 24 more signals were generated. These 36 signals are fed as input to the Mosfet driver of the multi-level inverter.

7.6 Discussions on FPGA development

Fig. 14 gives the Proposed Sequential Architecture for PDPWM. Fig. 15 gives the carrier frequency sampling module. Fig. 16 gives the reference carrier generation module and Fig. 17 illustrates the phase comparison module. The developed codes were using VHDL. Codes were simulated using modelsim and the codes were synthesized using Xilinx XST. Fig. 18 to 22 gives the simulation of phase disposition PWM using modelsim. After the simulation the codes were synthesized using

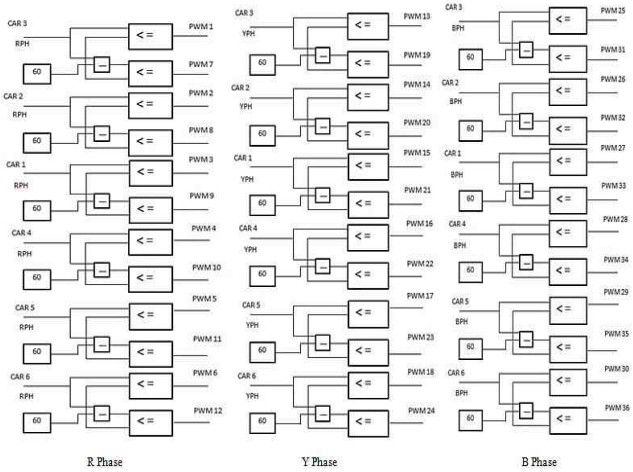


Fig. 17. Phase comparison module

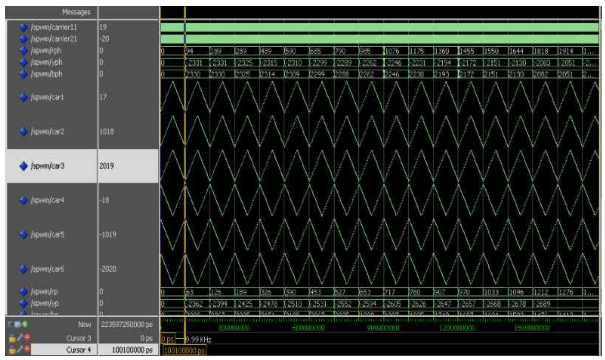


Fig. 18. FPGA Carrier Pulse for PD PWM using Modelsim

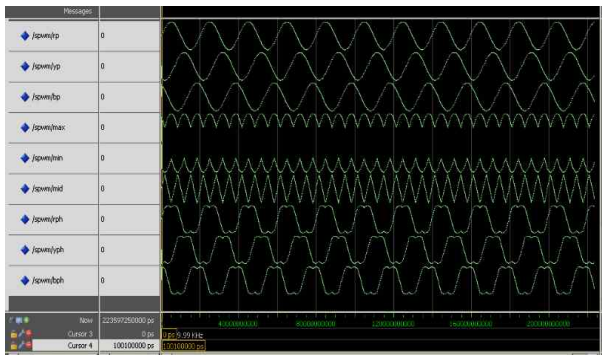


Fig. 19. FPGA carrier pulse reference waveform for PD PWM using modelsim

Xilinx XST. The codes were targeted for 6slx25ftg256-3 FPGA. Section 7 briefs with the device utilization summary of the developed VHDL code for phase disposition PWM. It was found that the developed architecture operates at 43.717 MHz, consumes 1105 slices.

7.7 Synthesis/Place and route report

Device utilization summary: Selected Device : 6slx25ftg256-3

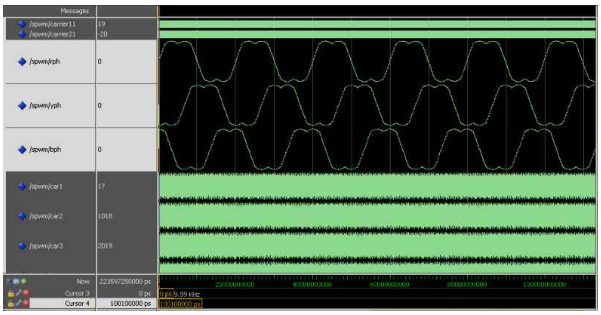


Fig. 20. FPGA Carrier – Reference Generation PD PWM using Modelsim

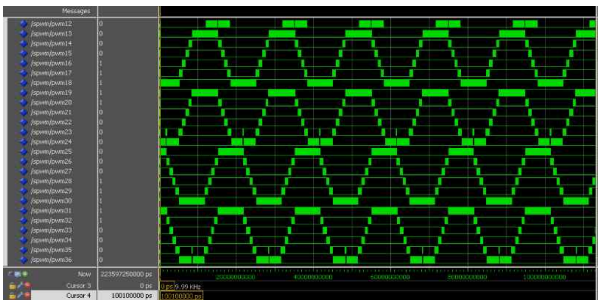


Fig. 21. FPGA PWM generation PD PWM using Modelsim

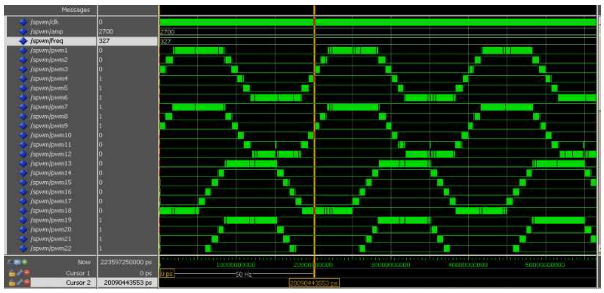


Fig. 22. FPGA Reference PD PWM using Modelsim

7.8 Slice Logic Utilization

Number of Slice Registers: :1105 out of 30064 (3%)
Number of Slice LUTs: 3479 out of 15032 23%
Number used as Logic: 3479 out of 15032 23%

7.9 Slice Logic Distribution (Space utilization are shown in percentage)

Number of LUT Flip Flop pairs used: 3766
Number with an unused Flip Flop: 2661 out of 3766 70%
Number with an unused LUT: 287 out of 3766 7%
Number of fully used LUT-FF pairs: 818 out of 3766 21%
Number of unique control sets:34

7.10 IO Utilization:

Number of IOs: 71
Number of bonded IOBs: 71 out of 186 38%
IOB Flip Flops/Latches: 1

7.11 Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%
Number of DSP48A1s: 18 out of 38 47%

7.12 Timing Summary:

Speed Grade: -3
Minimum period: 22.874ns
(Maximum Frequency: 43.717MHz)
Minimum input arrival time before clock: 10.180ns
Maximum output required time after clock: 3.597ns

8. Hardware Developed

In Fig. 23, the proposed three phase seven level diode clamped multilevel inverter is connected to induction motor. A speed sensor is connected to the shaft of the motor, latter encoded and given as input to the FPGA which acts as digital controller. HEDS5645 QEP Speed Sensor is used to Sense the Speed of Induction Motor. The Phase disposition (PDPWM) is implemented in FPGA. This digital controller (FPGA) will generate PWM based on the proportional integral control received from the sensor. These generated PWM is fed into the Mosfet of the proposed hardware circuits. It switches the Mosfet thereby the speed of the induction motor is controlled.

The following are the parameters considered for both simulation and hardware implementation of speed control of induction motor. Torque speed characteristics were performed

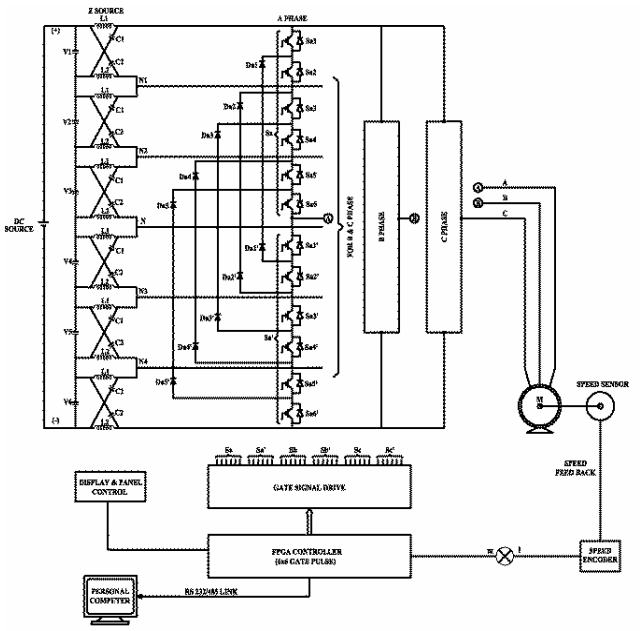


Fig. 23. Proposed hardware for Speed control of induction motor using PDPWM implemented on FPGA

- DC link voltage 300V DC
- Inverter power rating 200 W
- Inverter o/p voltage 0-200V AC RMS (line to line)
- Switching frequency 2000Hz
- NO OF CARRIER USED 6 Nos
- RATED POWER 0.25HP
- VOLTAGE 200VRMS
  (Ph-Ph)DELTA CONNECTION
- CURRENT 0.6A rms
- FREQUENCY 50Hz
- POLES 4Pole
- SYNCHRONOUS SPEED 1500RPM
- Rs 20.2OHM
- LS 0.032H
- Rr 8.02 OHM
- Lr 0.032H
- LM(mutual inductance) 0.601H
- Inertia(j) 0.0051

Fig. 24 and 25 illustrates the Power supply and wiring diagram of the proposed power circuit on a PCB. Fig. 26 gives the hardware set up used for conducting the speed characteristics of induction motor. Fig. 27 gives the snap shot of digital storage oscilloscope displaying PWM pulses generated. Figs. 28-31 gives the current THD, voltage THD, Phase voltage, phase current measured using THD meter respectively.

Table 4 illustrates the comparison of simulated and actual quantitative parameters for the proposed hardware circuit. During test on induction motor, THD meters were

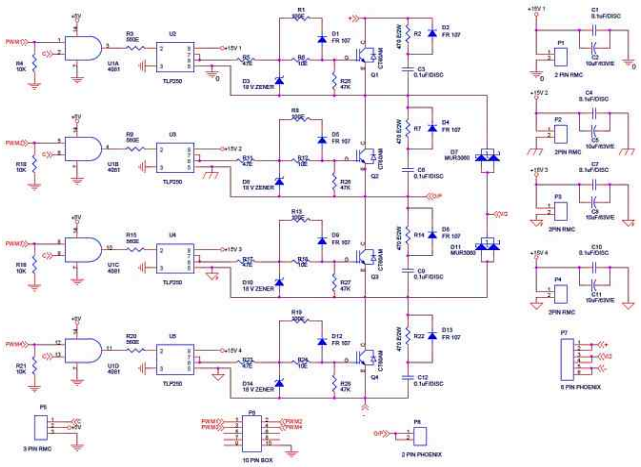


Fig. 24. Wiring diagram for Diode Clamped seven level Inverter – one leg

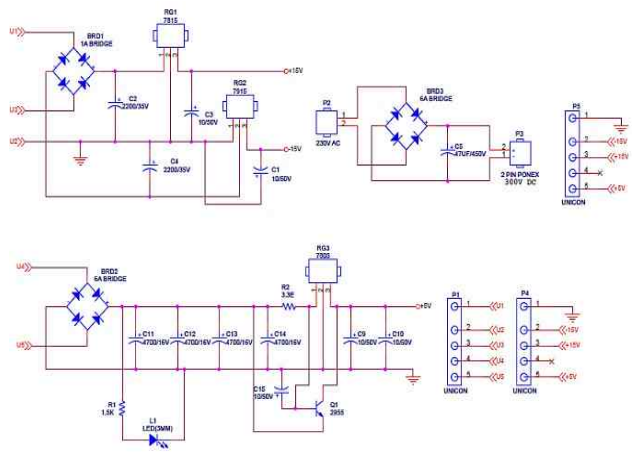


Fig. 25. Power supply unit for Diode Clamped seven level Inverter – one leg

Table 4. Comparison of simulated and actual quantitative parameters of the proposed hardware circuit

PWM	TYPE	PH(V) THD	L(V) THD	STA(I) THD	(V) STR	S[D SET(t)
PD	Simulation	29.98%	12.98%	1.55%	50V	0.2sec
	Actual	30.1%	13.7%	1.59%	50V	0.21 sec

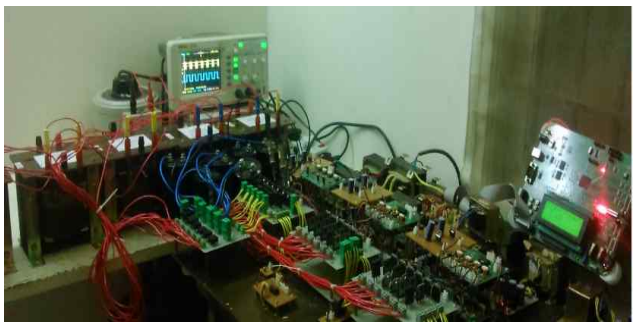


Fig. 26. Proposed hardware circuit set up

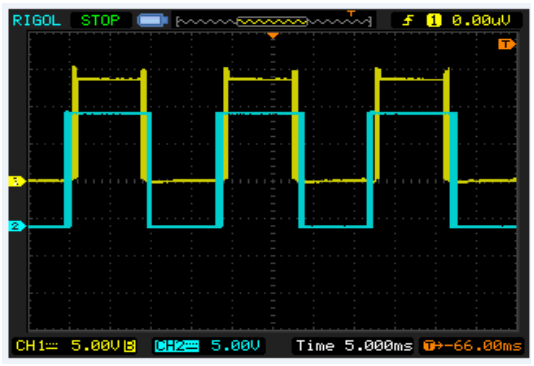


Fig. 27. PWM pulse generated from FPGA displayed in DSO

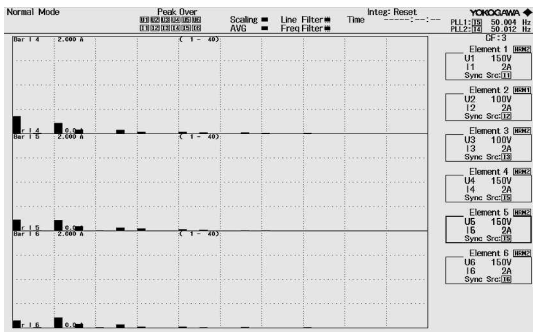


Fig. 28. Current THD measured using THD meter

Fig. 29. Voltage THD measured using THD meter

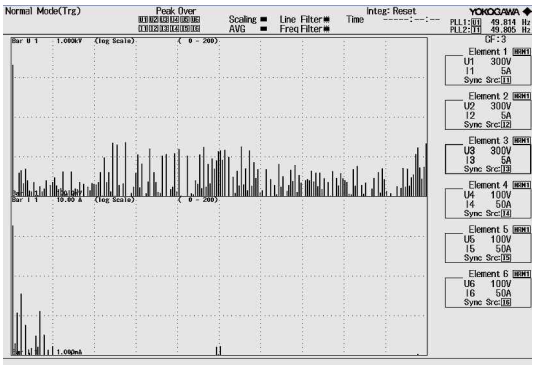


Fig. 30. Phase voltage THD measured using THD meter

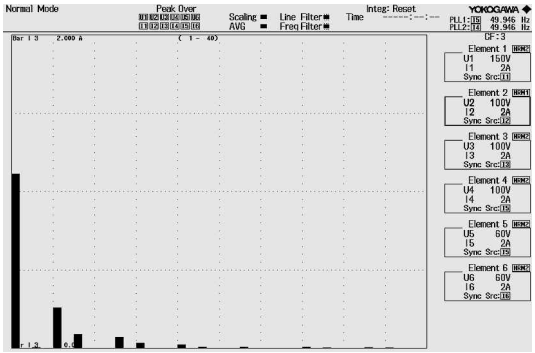


Fig. 31. Phase current THD measured using THD meter

used to acquire the required results and latter used for comparison. From Fig. 12 illustrates the performance of the proposed algorithm in terms of low THD values in comparison with other existing PWM techniques.

9. Conclusion

In this work, VLSI architecture for phase disposition PWM control was developed and tested in real time by connecting with induction motor. Speed control characteristics of the induction motor were performed. The performance of the proposed circuit was evaluated using THD, voltage stress and settling time. The same is validated using the real time measurements. From the analysis it is concluded that THD for PD PWM technique was found to exhibit low THD, creates less voltage stress and settles quickly when compared to other PWM schemes.

References

[1] R.G. Shriwastavaa, M.B. Daigavaneb, P.M. Daigavanec, "Simulation Analysis of Three Level Diode Clamped Multilevel Inverter Fed PMSM Drive Using Carrier Based Space Vector Pulse Width Modulation (CB-SVPWM)," *International Conference on Communication, Computing and Virtualization 2016, Procedia Computer Science,* vol. 79, pp. 616-623, June 2016.

[2] Swathy C. S., Reshma Ravi, Swetha K. S., "Study of Multilevel Inverter Topologies and Modulation Techniques," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 5, no. 3, pp. 1973-1978, March 2016.

[3] Pairote Thongprasri, "Capacitor balancing in DC link five level full bridge diode clamped multilevel inverter," *Indian Journal of pure and applied physics*, vol. 54, pp. 73-80, January 2016.

[4] Hammond, P.W., "Four-quadrant AC-AC drive and method," U.S. Patent 6 166 513, Dec.2000.

[5] Horn, A., Wilkinson, R.H. and Enslin, T.H.R., "Evaluation of converter topologies for improved power quality in DC traction substations," *in Proc. IEEE-ISIE*, pp. 802-807, June 1996.

[6] Joachim Holtz, "Optimal control of a dual three-level inverter system for medium-voltage drives," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, October 2008.

[7] Marchesoni, M., Mazzucchelli, M. and Tenconi, S., "A nonconventional power converter for plasma stabilization," *IEEE Trans. on Power Elect.*, vol. 5, no. 2, pp. 212-219, April 1990.

[8] Min, W., Min .J. and Choi, J., "Control of STATCOM using cascade multilevel inverter for high power application," *in Proc. IEEE-PEDS*, pp. 871-876, July 1999.

[9] Osman, R. H., "Medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," *in Proc. IEEE-IAS*, pp. 2662-2669, October 1999.

[10] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A New Medium Voltage PWM Inverter Topology for Adjustable Speed Drives," *in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO*, pp. 1416-1423, June 1999.

[11] H. L. Liu, G. H. Cho, "Three-Level Space Vector PWM in Low Index Modulation Region Avoiding Narrow Pulse Problem," *IEEE Transactions on Power Electronics*, vol. 9, no. 5, pp. 481-486, September 1994.

[12] Sanoop P, Vinita Chellappan, "Seven Level Inverter Topologies: A Comparative Study," *International Journal of Innovative Research in Electrical, Elec-*

tronics and Instrumentation and Control Engineering, vol. 3, Special no. 1, pp. 148-160, February 2016.
[13] Usha V, Pavitha S, Shanmathy M, "Advanced Harmonic Elimination Techniques analysis for various Neutral Point Clamped Inverter Fed Induction Motor drives," *International Journal of Advanced Research in Education & Technology*, vol. 4, no. 2, pp. 191-195, June 2017.
[14] B.S. Jin, W.K. Lee, T.J. Kim, D.W. Kang, and D.S. Hyun, "A Study on the multi carrier PWM methods for voltage balancing of flying capacitor in the flying capacitor multilevel inverter," *in proc. IEEE Ind. Electron.Conf*., pp. 721-726, November 2005.
[15] Ki-Seon Kim, Young-Gook Jung, and Young-Cheol Lim, Member, IEEE "A New Hybrid Random PWM Scheme," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, January 2009.

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