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Level Number Effect on Performance of A Novel Series Active Power Filter Based on Multilevel Inverter

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Abstract – This paper presents a single-phase asymmetric half-bridge cascaded multilevel inverter based series active power filter (SAPF) for harmonic voltage compensation. The effect of level number on performance of the proposed SAPF is examined in terms of total harmonic distortion (THD) and system efficiency. Besides, the relationship between the level number and the number of switching device are compared with the other multilevel inverter topologies used in APF applications. The paper is also aimed to demonstrate the capability of the SAPF for compensating harmonic voltages alone, without using a passive power filter (PPF). To obtain the required output voltage, a new switching algorithm is developed. The proposed SAPF with levels of 7, 15 and 31 is used in both simulation and experimental studies and the harmonic voltages of the load connected to the point of common coupling (PCC) is compensated under two different loading conditions. Furthermore, very high system efficiency values such as 98.74% and 96.84% are measured in the experimental studies and all THD values are brought into compliance with the IEEE-519 Standard. As a result, by increasing the level number of the inverter, lower THD values can be obtained even under high harmonic distortion levels while system efficiency almost remains the same.

Keywords: Active power filter, Multilevel inverter, Harmonics, Total harmonic distortion, Power quality, System efficiency

1. Introduction

Rapid increase in the number of non-linear loads causes a power quality deterioration in electric transmission and distribution systems, due to harmonics. The non-linear load drawing harmonic current results in the deformation of the source voltage waveform at the point of common coupling (PCC). This leads to a non-sinusoidal source voltage for other loads connected to the PCC. Conventionally, passive power filters (PPFs) have been used in order to suppress harmonics. However, they are inadequate and have adverse influences. They may produce resonance and their performance is strongly affected by the network impedance. In addition, they are bulky, and have fixed compensating characteristic as they are designed for a specific frequency [1-3]. In order to overcome these drawbacks, active power filtering becomes an important area of concern for filtering harmonics and researches are intensified to this topic in last decades.

Active power filters (APFs), which can be applied to solve many problems such as filtering harmonics, reactive power compensation, resonance suppression and voltage regulation, are basically classified as follows according to the connection to the system: parallel active power filter (PAPF) and series active power filter (SAPF). Most of the APFs have been proposed until now are of parallel type [4-7]. Their performance is better in compensating harmonic current produced by non-linear load acting as a harmonic current source. SAPFs are more effective to compensate harmonic voltages. Several SAPFs have been proposed, and most of them operate in a hybrid way with shunt PPF [8-11]. In hybrid topologies, the inverter capacity of the filter is reduced and the disadvantages of the PPF is mitigated.

With multilevel inverters, lower total harmonic distortion values can be achieved at the inverter output. In addition, any harmonic output waveform can be produced by multilevel inverters. Thus, APFs based on various topologies of multilevel inverters have been proposed in the literature. These topologies are classified as diode-clamped multilevel inverters [12-13], multilevel inverters with flying capacitor [14] and H-bridge cascaded multilevel inverters. The H-bridge cascaded multilevel inverter (HCMLI) topology in APFs is preferred more than others [15-18]. To be applicable in high voltage and power, to achieve reduced dv/dt ratio on switching devices, to use lower numbers of semiconductor switching devices and to have output voltage with lower harmonic levels are the main reasons for this preference. The proposed SAPF based on a half-bridge cascaded multilevel inverter has all the advantages of HCMLI topologies. The topology used in the proposed SAPF is more advantageous than the topologies mentioned before since the same level of the output voltage can be

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achieved by using lower number of semiconductor switching devices. The easy acquisition of switching signals for the switching devices simplifies the structure of the control system. The simplicity of the control system is also an important advantages of the proposed SAPF.

In this paper, a single-phase multilevel inverter based SAPF is proposed to represent the effect of level number on the inverter performance by means of THD value and system efficiency. The paper is also aimed to demonstrate the capability of the SAPF for compensating harmonic voltages alone, without using a PPF. Therefore, the structure of the half-bridge cascaded multilevel inverter used in the proposed SAPF and its operating principle are presented comprehensively in Section II. The experimental setup is realized in a simulation study. The simulation results are presented in Section III. In Section IV, the experimental results are given. Additionally, the value of the system efficiency is presented for both simulation and experimental studies.

2. Structure and Operating Principle of the Proposed SAPF

A schematic diagram of the experimental setup for the proposed SAPF based on a multilevel inverter is shown in Fig. 1. The non-linear load consists of a single-phase diode rectifier with an RC load at the dc side. The harmonic currents drawn by the non-linear load cause harmonic voltage on the resistor R_s which is in series with the sinusoidal voltage source V_s. Due to the harmonic voltage on R_s, there is a distortion in the waveform of the PCC voltage. A linear load, hereafter referred to as the load, connected to the PCC is now fed by a non-sinusoidal voltage (PCC and F are the same points before connecting the series active power filter). The harmonic components of the load voltage are eliminated by the proposed SAPF based on the multilevel inverter located between the load and the PCC. The voltage and current sensors are available in the experimental setup to measure the voltage and current at the PCC. In addition, a Zero-Crossing Detector (ZCD) is designed to synchronize with the phase angle of the voltage source V_s, and it is placed into the experimental setup. As shown in Fig. 1, the number of level modules can be changed. The purpose of this study is to examine the effect of level number on THD and system efficiency by increasing the number of level modules.

2.1 Structure of the Multilevel Inverter

The proposed SAPF has a single-phase multilevel inverter. The multilevel inverter is composed of two main parts. The H-Bridge Module (HM), which is conventionally used in multilevel inverters, is the constant part of the multilevel inverter. The other part is called as Level Module (LM). The LMs are connected in series to increase the number of output levels of the multilevel inverter.

In Fig. 2, the structure of an LM is shown. An LM comprises a dc source and two semiconductor switching devices. The voltage of the dc source V_d in LM_1 is determined by the required maximum value of the output voltage and the level of the inverter as;

$$V_d = \frac{2V\max}{n-1} \quad (1)$$

where V_{max} is the required maximum value of the output voltage, and n is the level of the inverter. n can be expressed as;

$$n = 2^{m+1} - 1 \quad (2)$$

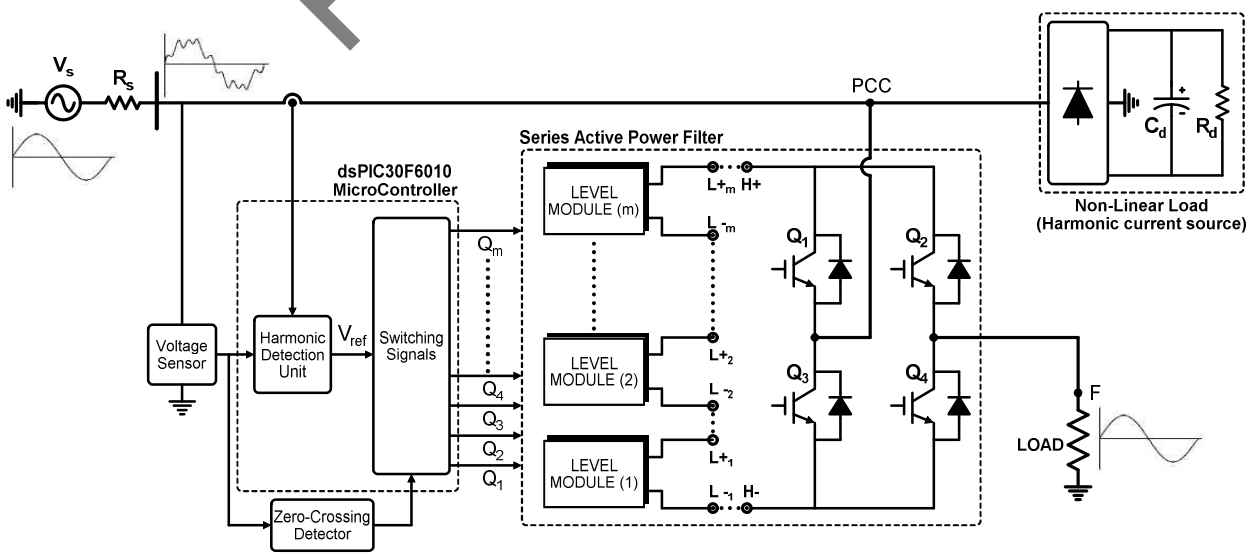


Fig. 1. Schematic diagram of the experimental setup for the proposed SAPF

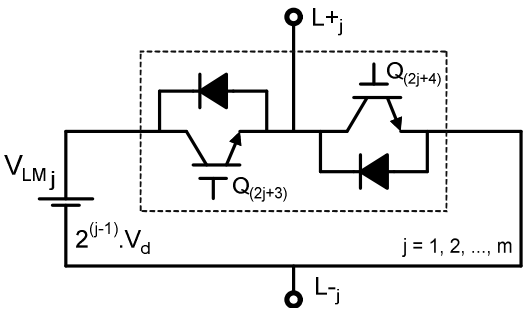


Fig. 2. Structure of a level module

where m is the number of LMs used in the inverter.

The multilevel inverter has an asymmetric structure since the voltage of the dc sources in the LMs are scaled in power of 2 which can be seen from Fig. 2.

The value of n is the maximum level number of the inverter. Accordingly, up to 31-level can be achieved by four LMs. However, any required number of level such as 17, 21 or 27 can also be obtained by four LMs. By increasing the number of LMs, any required number of level can be easily obtained by the proposed inverter since it has a simple and modular structure.

The number of semiconductor switching devices r used in the proposed inverter can be computed according to m as follows;

$$r = 2m + 4 \tag{3}$$

The structure of the multilevel inverter used in the proposed SAPF is more advantageous than the topologies mentioned before since the same level of the output voltage can be achieved by using lower number of semiconductor switching devices. To illustrate this advantage, the proposed inverter structure is compared with other multilevel inverter topologies used in APF applications. Only the topologies of HCMLIs are compared with the proposed inverter in the Table 1, since the diode-clamped multilevel inverters and the multilevel inverters with flying-capacitor necessitate too many clamping-diodes and flying-capacitors, which cause lower efficiencies, apart from the switching devices [12-14]. The topology of Cascaded-1 is a symmetric HCMLI with equal dc sources in each cascaded module [15-16], while the Cascaded-2 and Cascaded-3 are asymmetric [17-18]. If at least one of the dc sources in the cascaded modules is different from the others then the inverter is called asymmetric. By using the same number of switching devices, asymmetric inverters can achieve a higher voltage magnitude and level at the output. In Cascaded-2, the dc sources in the modules scaled in power of 2 provide the asymmetry [17]. The turn ratio of the interfacing transformers in Cascaded-3 are scaled in power of 3 [18]. The proposed inverter structure is also asymmetric and more advantageous than asymmetric HCMLIs in terms of the number of switching devices.

In Table 1, the inverter level and the number of switching devices are compared for an inverter with m-modules. The results of the comparison made for the inverter topologies in Table 1 can be summarized as follows:

Table 1. The numbers of level and the switching devices for a single-phase multilevel inverter with m level modules

Topology	Number of Level / Number of Switches	Number of level module (m) 2	3	4	5	6	…	m
Cascaded-1	n	5	7	9	11	13	…	2m+1
	r	8	12	16	20	24	…	4m
Cascaded-2	n	7	15	31	63	127	…	$2^{(m+1)}$-1
	r	8	12	16	20	24	…	4m
Cascaded-3	n	9	27	81	243	729	…	3^m
	r	8	12	16	20	24	…	4m
Proposed	n	7	15	31	63	127	…	$2^{(m+1)}$-1
	r	8	10	12	14	16	…	2m+4

1) For a determined level number, for example n= 63, Cascaded-1, Cascaded-2 and the proposed inverter topology have to use 124, 20 and 14 switching devices, respectively.

As can be seen in Table 1, the topology of Cascaded-3 requires at least 16 switching devices for the same level to be achieved. Hence, the proposed inverter topology is the most advantageous topology depending on the number of switching devices for a determined level number. The number of switching devices is a parameter that directly affects switching losses. Therefore, the lower number of switching devices reduces switching losses in continuous current. In addition, the lower number of switching devices significantly reduces the costs for medium and high voltage levels.

ii) If the inverters in Table 1 are designed with the same number of switching devices, for example r=12, Cascaded-1, Cascaded-2 and Cascaded-3 topologies can respectively provide 7, 15 and 27 level at the output. And, a 31-level output voltage waveform can be achieved with the proposed inverter topology. Therefore, if the inverters in the table are compared for the same number of switching devices, the proposed inverter topology achieves a higher level number at the output.

Table 1 shows that the number of switching devices in the proposed inverter is directly proportional to the number of level. However, due to conduction and switching losses, the number of switching device is inversely proportional to the efficiency of the system. Simulation and experimental studies are carried out to show this and a table is created to show how the system efficiency changes depending on the number of levels in Section 4.

2.2 Operating principle

The multilevel inverter used in the proposed SAPF has the capability to generate an output voltage waveform more sinusoidally. Furthermore, the multilevel inverter

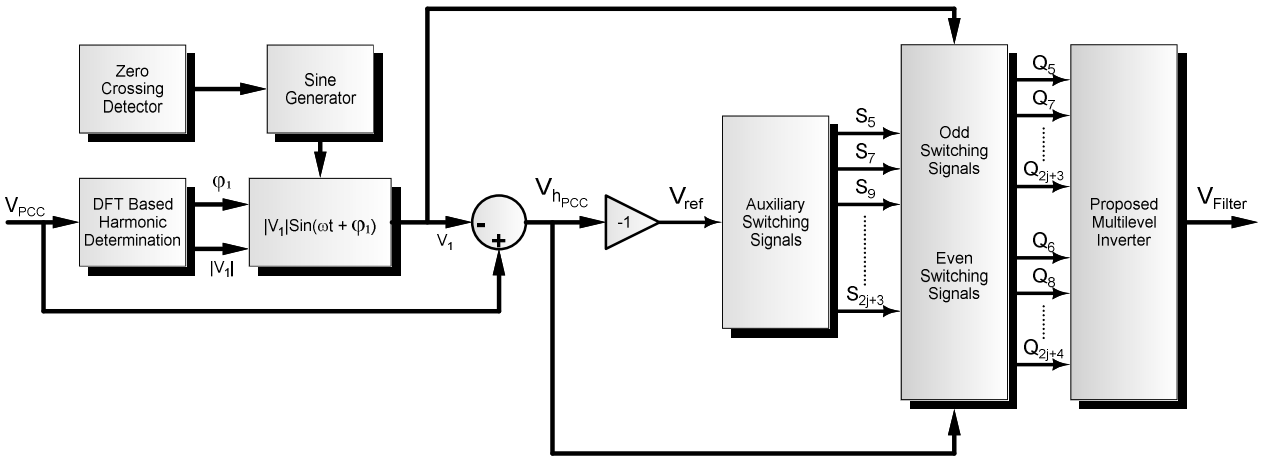


Fig. 3. Block diagram of the control algorithm

can produce any voltage with harmonic components. Due to this feature, it acts as a harmonic voltage source.

The block diagram of the control algorithm used to calculate the active filter compensation voltage (V_{Filter}) is shown in Fig. 3. Initially, the measured analog voltage and current at the PCC are sampled by means of the analog-to-digital converter (ADC) in the microcontroller. In the harmonic detection unit, the microcontroller then performs an algorithm based on Discrete Fourier Transform (DFT) to obtain the spectrum of the sampled waveforms. The DFT is defined as;

$$w_h = \frac{2\pi}{N} h, \qquad 0 \le \mathrm{h} \le (\mathrm{N}\text{-}1) \tag{4}$$

$$V_h = \sum_{n=0}^{N-1} v(n) e^{-jw_h n} \tag{5}$$

where N is the number of samples, V_h is the harmonic spectrum and $v(n)$ are the input samples. Computing only the fundamental harmonic according to Eq. (5) is adequate to obtain the reference voltage signal. The following equations formulates the way used to determine the reference voltage signal. When the fundamental harmonic voltage is subtracted from the PCC voltage, the inverse of the remaining voltage represents the reference.

$$V_{h_{PCC}}(t) = \sum_{h=2}^{\infty} V_h \sin(h\omega t + \phi_h) \tag{6}$$

$$V_{h_{PCC}}(t) = V_{PCC}(t) - V_1 \sin(\omega t + \phi_1) \tag{7}$$

$$V_{ref}(t) = -V_{h_{PCC}}(t) \tag{8}$$

The obtained reference voltage is expressed as shown in Eq. (8). After determining V_{ref}, it is simple to find the switching signals. The instantaneous values of the reference voltage for each sampling are substituted in Eq. (9) to calculate S values (auxiliary switching signals) for j =1,2,3,...,m. The auxiliary switching signals are then substituted into the generalized formulas as represented in Eq. (10) and Eq. (11) to determine the switching signals for the switching devices used in LMs. The control scheme used to determine the odd switching signals of the proposed inverter with a number of level modules m is illustrated in Fig. 4.

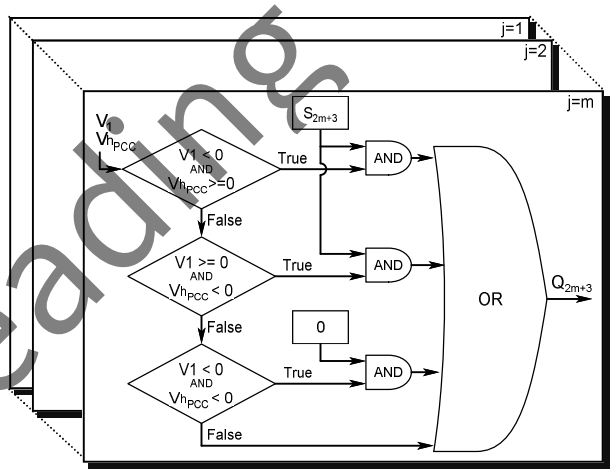
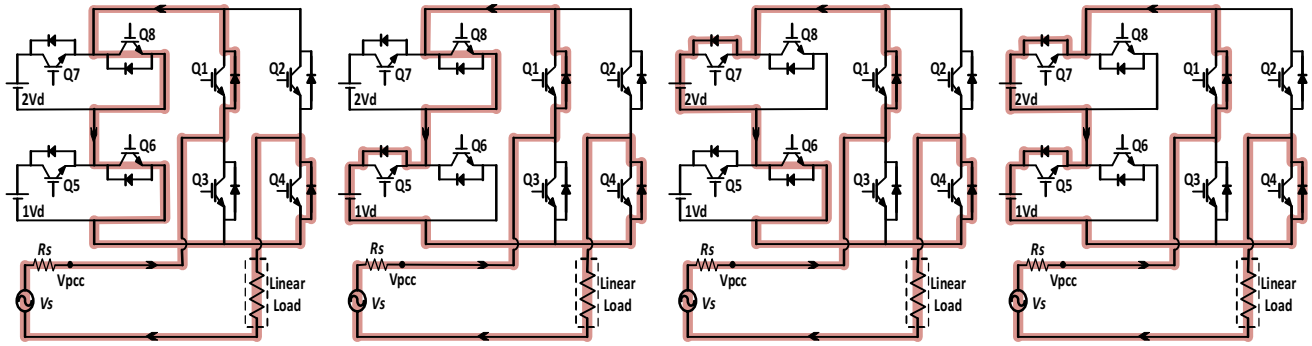


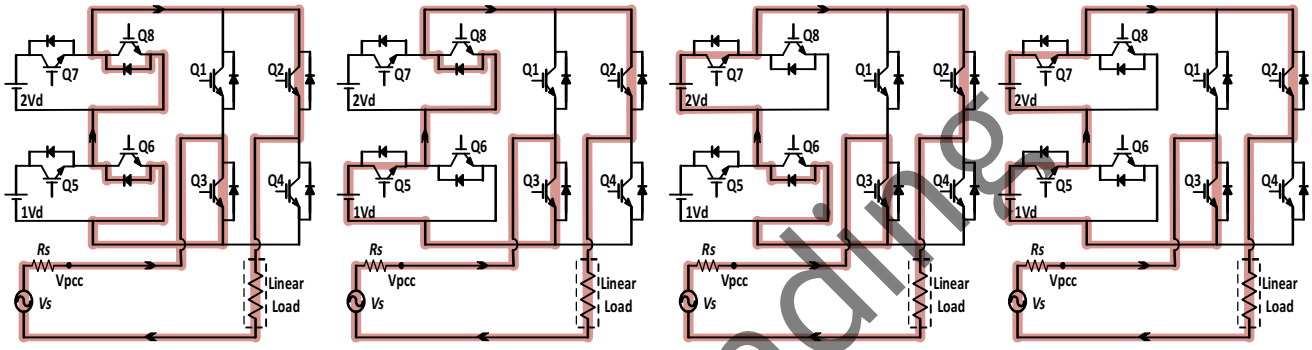
Fig. 4. Odd switching signals determination

$$S_{2j+3}(t) = \left[\frac{V_{ref}(t) - V_{ref}(t) \bmod 2^{j-1}}{2^{j-1}} \right] \bmod 2 \tag{9}$$

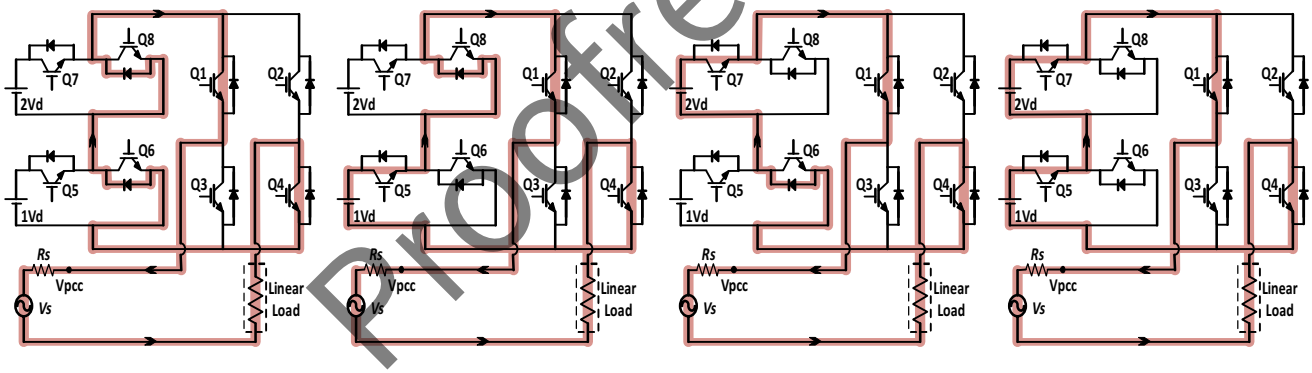
$$Q_{2j+3}(t) = \begin{cases} 0, & (V_1 \ge 0 \wedge \sum_{h=2}^{\infty} V_h \ge 0) \\ 0, & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ S_{2j+3}(t), & (V_1 \ge 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ S_{2j+3}(t), & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h \ge 0) \end{cases} \tag{10}$$



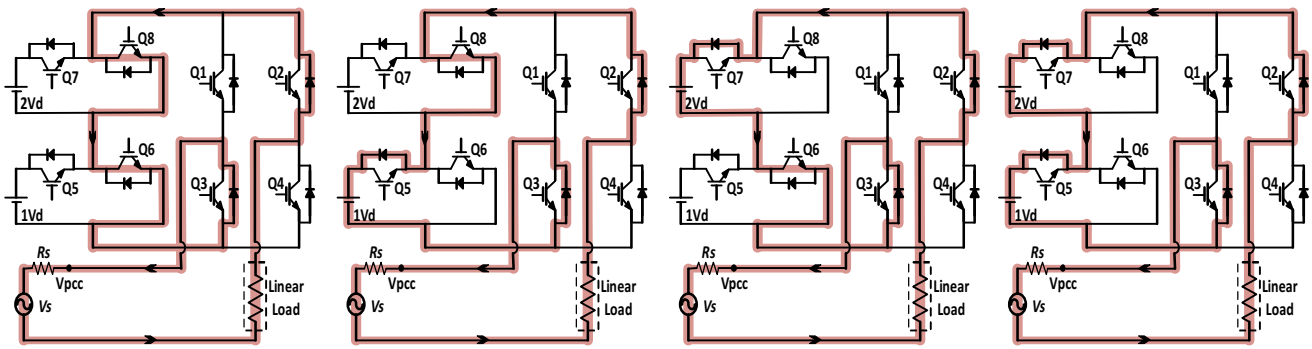
(a)$V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inv} = 0$) (b)$V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inv} = -V_d$) (c)$V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inv} = -2V_d$) (d)$V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inv} = -3V_d$)



(e)$V_1 \geq 0$, $\sum V_h < 0$ ($V_{inv} = 0$) (f)$V_1 \geq 0$, $\sum V_h < 0$ ($V_{inv} = -V_d$) (g)$V_1 \geq 0$, $\sum V_h < 0$ ($V_{inv} = -2V_d$) (h)$V_1 \geq 0$, $\sum V_h < 0$ ($V_{inv} = -3V_d$)



(i)$V_1 < 0$, $\sum V_h \geq 0$ ($V_{inv} = 0$) (j)$V_1 < 0$, $\sum V_h \geq 0$ ($V_{inv} = -V_d$) (k)$V_1 < 0$, $\sum V_h \geq 0$ ($V_{inv} = -2V_d$) (l)$V_1 < 0$, $\sum V_h \geq 0$ ($V_{inv} = -3V_d$)



(m)$V_1 < 0$, $\sum V_h < 0$ ($V_{inv} = 0$) (n)$V_1 < 0$, $\sum V_h < 0$ ($V_{inv} = -V_d$) (o)$V_1 < 0$, $\sum V_h < 0$ ($V_{inv} = -2V_d$) (p)$V_1 < 0$, $\sum V_h < 0$ ($V_{inv} = -3V_d$)

Fig. 5. Operational modes of 7-level inverter based series active power filter under different characteristic states

$$Q_{2j+4}(t)=\begin{cases}\overline{S_{2j+3}(t)}, & (V_1\geq 0 \wedge \sum_{h=2}^{\infty} V_h \geq 0)\\ \overline{S_{2j+3}(t)}, & (V_1<0 \wedge \sum_{h=2}^{\infty} V_h<0)\\ 0, & (V_1\geq 0 \wedge \sum_{h=2}^{\infty} V_h<0)\\ 0, & (V_1<0 \wedge \sum_{h=2}^{\infty} V_h\geq 0)\end{cases} \quad (11)$$

In order to calculate the switching signals correctly, the instantaneous values of the reference voltage V_{ref} must be properly obtained. Therefore, the scan time should be chosen small enough. The scan time is the interval between two consecutive values of time. The maximum value of the scan time depends on the fundamental frequency and the number of LMs. It is crucial that the sample time should be chosen very small with respect to the maximum value of the scan time [19-21].

It can be seen from the above equations, it is very easy to obtain switching signals in the proposed multilevel inverter topology. Since the values of the dc sources used in LMs vary as the exponents of 2, binary representation of the reference voltage absolute value obtained instantaneously after the harmonic detection process gives the switching signals of each switching devices in LMs. The easy acquisition of switching signals simplifies the structure of the control system. The simplicity of the control system is one of the most important advantages of the proposed multilevel inverter topology, which makes it attractive for use in SAPF applications.

The switching signals of the multilevel inverter are obtained according to four different characteristic states as can be seen in Eq. (10) and Eq. (11). In the proposed SAPF, an inverter consisting two LMs can operate in a way of 7 different modes. All of the operational modes of the proposed SAPF are shown in Fig. 5. For example, to obtain a voltage level of $-2V_d$ under the characteristic state of ($V1\geq 0$ and $\sum V_h<0$), Q_2, Q_3, D_6, and Q_7 need to be used as shown in Fig. 5(g).

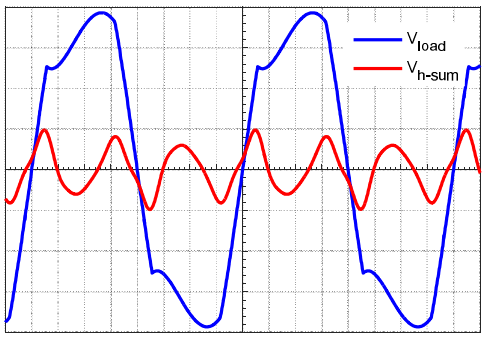
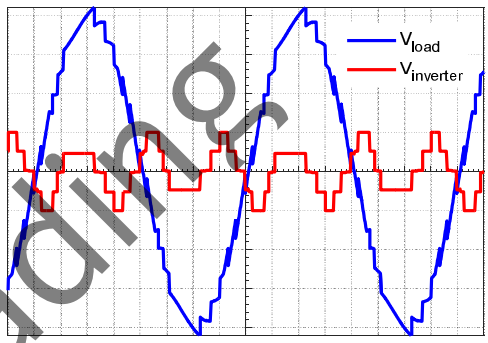


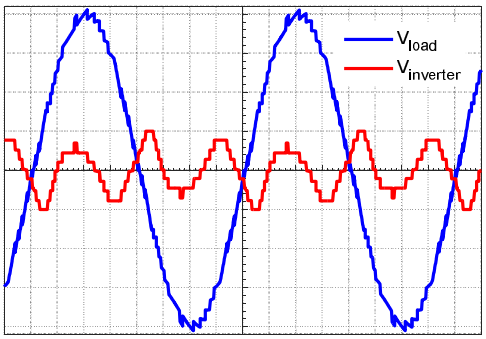
Fig. 6. The waveforms of the load voltage and its total harmonic components for Config.1 without SAPF (50 V/div, 2.5 ms/div)

3. Simulation Results

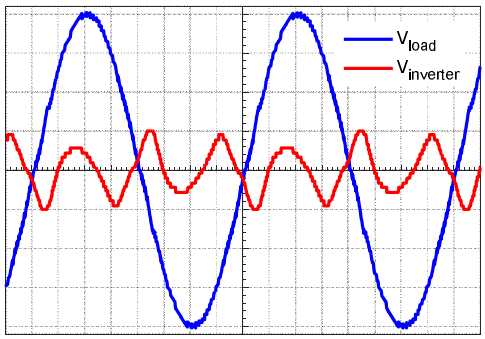
The proposed SAPF model based on the multilevel inverter is developed for the simulation arrangement as shown in Fig. 1. The SAPF simulation model is tested for compensating the harmonic voltages of the load at the PCC. To supply a high distorted voltage at the PCC, a resistor R_s is connected in series with the voltage source V_s. Configurations of circuit parameters leading to two different harmonic distortion levels are used to perform



(a) 7-level



(b) 15-level



(c) 31-level

Fig. 7. The waveforms of the load voltage and inverter output voltage for Config.1 using SAPF with levels of 7, 15 and 31 (50 V/div, 2.5 ms/div)

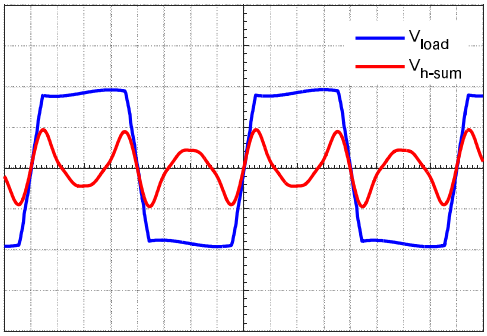
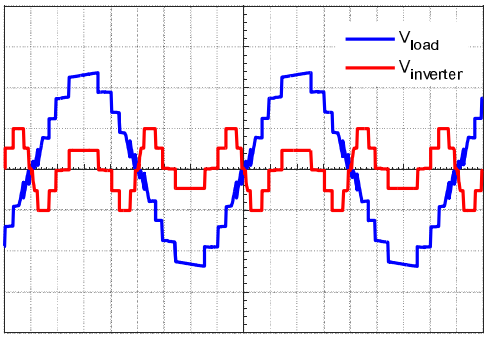
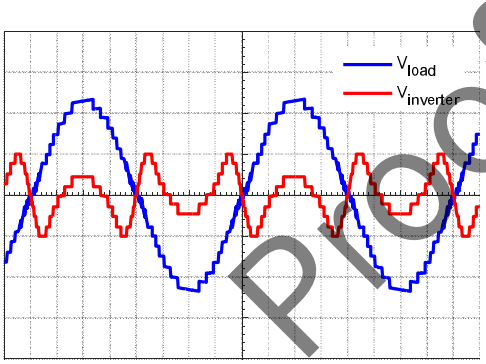


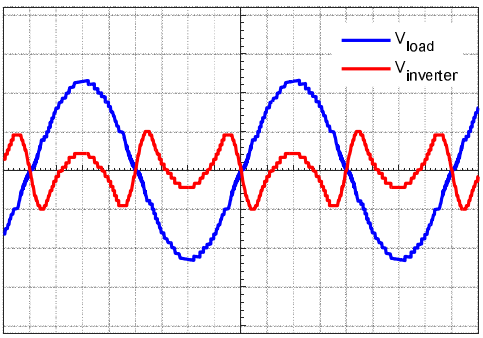
Fig. 8. The waveforms of the load voltage and its total harmonic components for Config.2 without SAPF (50V/div, 2.5 ms/div)



(a) 7-level



(b) 15-level



(c) 31-level

Fig. 9. The waveforms of the load voltage and inverter output voltage for Config.2 using SAPF with levels of 7, 15 and 31 (50 V/div, 2.5 ms/div)

Table 2. The THD values of the load voltage for both simulation and experimental studies

	Config.1		Config.2	
	Simulation	Experimental	Simulation	Experimental
Without SAPF	18.47%	18.30%	30.70%	29.81%
SAPF with 2 LMs (n =7)	4.65%	3.19%	8.09%	4.76%
SAPF with 3 LMs (n =15)	2.85%	2.24%	4.69%	2.76%
SAPF with 4 LMs (n =31)	1.90%	1.81%	3.43%	2.48%

the simulations. The configurations of circuit parameters, called as Config.1 and Config.2, are (R_s=16 Ω, R_d=48 Ω, C_d=204 μF, $Load$=192 Ω) and (R_s=192 Ω, R_d=192 Ω, C_d=204 μF, $Load$= 576 Ω), respectively. Additionally, the values of V_d are taken as 24V, 12V and 6V respectively for 7, 15 and 31-level inverters. For each distortion level, the SAPF simulation models with 2, 3 and 4 LMs are applied to compensate the harmonic voltages of the load.

The waveforms of the load voltage and its total harmonic components for each configuration obtained from simulations are shown in Fig. 6 and Fig. 8.

The harmonic components of the load voltage at the PCC are detected by the harmonic detection unit. The reference voltage function is constituted related to the detected harmonic components and the switching signals are generated. Simulations are carried out for the multilevel inverters with three different levels.

The waveforms of the load voltage and inverter output voltage for each configuration using SAPF with levels of 7, 15 and 31 are shown in Fig. 7 and Fig. 9, respectively. It can be seen from the simulation results shown in Fig. 7 and Fig. 9 that the inverter output voltage is achieved more convergent to the reference voltage as the number of LMs is increased. The more convergent the reference voltage, the lower THD value is obtained. In Table 2, the THD values of the load voltage are displayed depending on the number of LMs and configuration of circuit parameters.

4. Experimental Results

A prototype is developed on the basis of the system configuration shown in Fig. 1 to demonstrate the validity of the proposed SAPF based on the multilevel inverter. A photograph of the multilevel inverter is given in Fig. 11. There are six LMs in the photograph. However, the first 2, 3 or 4 LMs are used to constitute the levels of 7, 15 and 31, respectively. As it is intended to examine the effect of level number on THD and system efficiency, a prototype with up to four LMs is used. The prototype is implemented for a 220 V, 50 Hz, single-phase system. The single-phase half-bridge cascaded multilevel inverter consists of Mitsubishi IGBT modules and drivers with base boards. The digital controller dsPIC30F6010 is a 16-bit microcontroller from

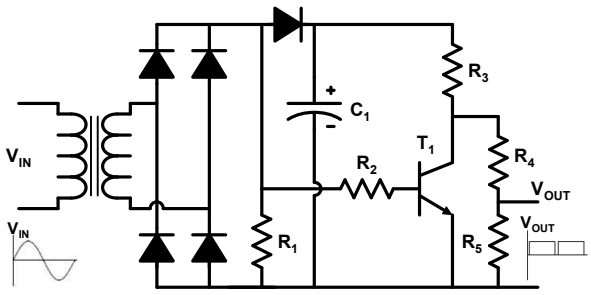


Fig. 10. The scheme of Zero-Crossing Detector (ZCD)

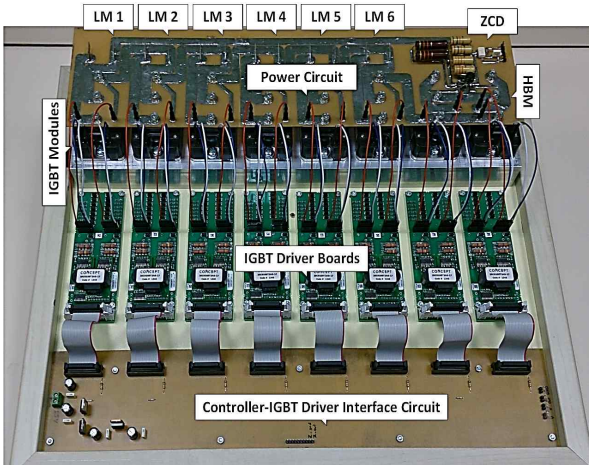


Fig. 11. The photograph of the multilevel inverter used in the proposed SAPF

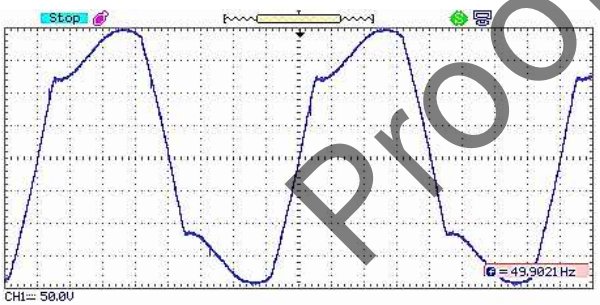
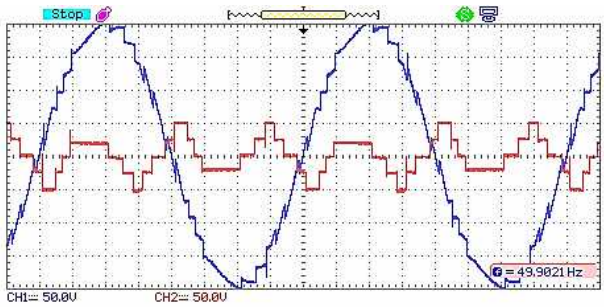


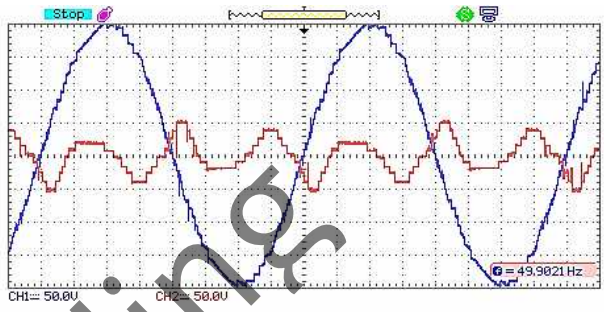
Fig. 12. The waveform of the load voltage for Config.1 without SAPF (50 V/div, 2.5 ms/div)

Microchip for high performance applications. The scheme of Zero-Crossing Detector (ZCD) seen in Fig. 10 is designed to generate a synchronized pulse related to the phase angle of the voltage source V_s. The ZCD detects the transition of the voltage source waveform from positive to negative (and vice versa), providing zero voltage. The output of this detector is connected to the external interrupt input of the microcontroller that is programmed as falling edge. In this way, it resets an existing timer that provides the synchronization each time the microcontroller detects an interrupt.

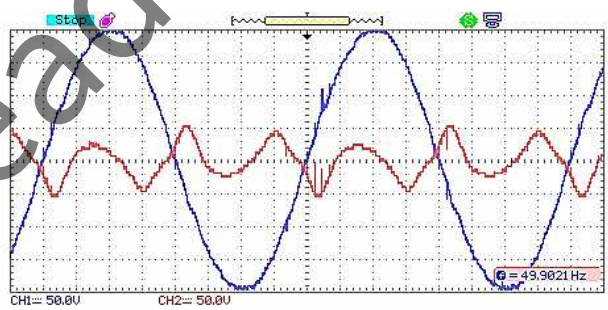
The SAPF experimental setup is tested for compensating



(a) 7-level



(b) 15-level



(c) 31-level

Fig. 13. The waveforms of the load voltage (CH1) and inverter output voltage (CH2) for Config.1 using SAPF with levels of 7, 15 and 31 (50 V/div, 2.5 ms/div)

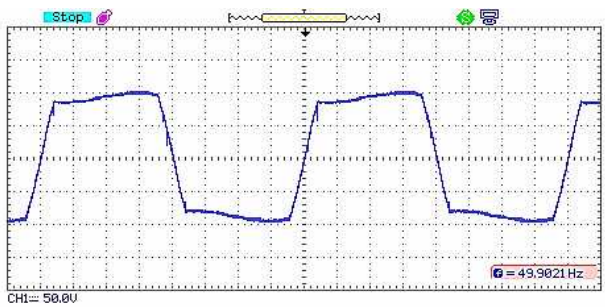
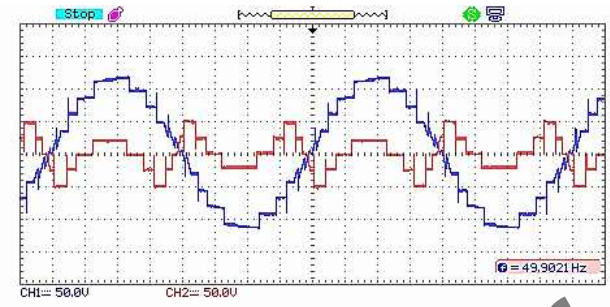


Fig. 14. The waveform of the load voltage for Config.2 without SAPF (50 V/div, 2.5 ms/div)

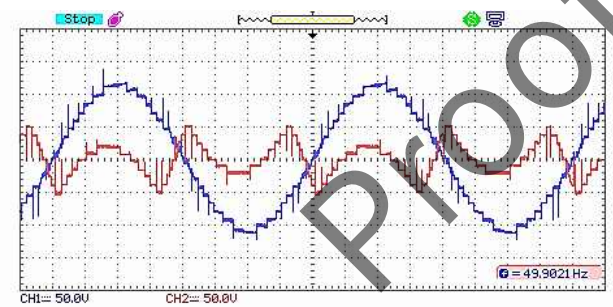
the harmonic voltages of the load connected to the PCC with the same configurations of circuit parameters used in the simulation study, and results are presented in Fig. 12,

Fig. 13, Fig. 14 and Fig. 15. The waveforms of the load voltage without SAPF are given in Fig. 12 and Fig. 14. The voltage waveforms of the load and the inverter output using SAPF with levels of 7, 15 and 31 are shown in Fig. 13 and Fig. 15. The THD values of the load voltage for Config.1 and Config.2 with/without SAPF are displayed in Table 2 compared with simulation results.

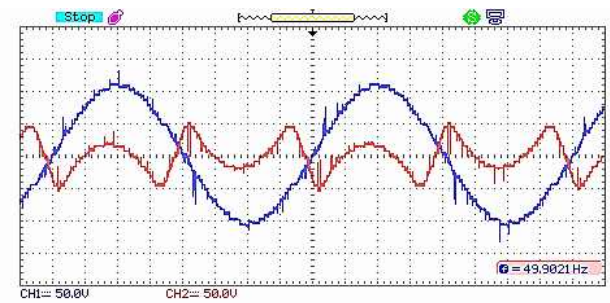
It is clear that the THD value of the load voltage is reduced significantly for all of the parameter configurations. A comparison between the THD values with/without SAPF can be easily done for the simulation and experimental studies. For example, the distortion level from the simulation and experimental studies can be seen respectively in Fig. 6 and Fig. 12 for Config.1 before compensation. After compensation, the THD value of load voltage is significantly decreased from 18.47% to 4.65%, 2.85% and 1.90% by using SAPF with levels of 7, 15 and 31, respectively for the simulation study. The THD value of 30.70% for the experimental study is reduced to 8.09%, 4.69% and 3.43% by using SAPF with the same levels used in the simulation study. For both configurations, the load voltage is nearly sinusoidal as seen in Fig. 7 and Fig. 9 for the simulation, and in Fig. 13 and Fig. 14 for the experiments.



(a) 7-level



(b) 15-level



(c) 31-level

Fig. 15. The waveforms of the load voltage (CH1) and inverter output voltage (CH2) for Config.2 using SAPF with levels of 7, 15 and 31 (50 V/div, 2.5 ms/div)

The inverter topology used in the proposed SAPF has advantages over the multilevel inverter topologies used in APF applications according to switchings losses. Using lower number of semiconductor switching devices reduces the switching losses in the continuous current. In addition, the switchings frequency in the proposed SAPF is much lower than those of PWM inverter based APFs. PWM inverters used conventionally in APF applications operate with a switching frequencies of 15-23 kHz [1, 2, 6, 14, 22, 23]. High-order harmonics and additional switching losses occur in PWM inverters operating at such high frequencies [8]. The switching frequency can be expressed as a parameter that affects the system efficiency, since the low switching frequency reduces the switching losses which cause the increase in the system efficiency. The multilevel inverter used in the proposed SAPF operates at lower frequencies. In the proposed SAPF, the multilevel inverters with the number of level modules (m) 2, 3 and 4 are used in both simulation and experimental studies. The switching devices in each level modules operates at different switching frequencies. For instance, the most significant module operates at the frequency of 500 Hz in a 3-level module inverter, while the other two modules operate at the frequencies of 2 kHz and 3 kHz to obtain a fifth harmonic at the inverter output. Furthermore, there is no need for the filter circuits which are used at the output of the PWM inverters to make output voltage sinusoidal. Advantages of lower number of semiconductor switching devices, lower switching frequencies and no filter requirement are the parameters that makes the system efficiency higher. In Table 3, the system efficiency of the proposed asymmetric half-bridge cascaded multilevel inverter based SAPF is given through simulation and experimental study using the configurations of circuitparameters. As seen in Table 3, the system efficiency is not affected significantly despite the increase in the number of level. The system efficiency is decreased from 97.84% to 96.81% in simulation and from 96.84% to 94.87% in experimental study, although the number of switching devices increased only by 4 which leads to a higher level number.

Table 3. System Efficiency of the proposed SAPF

	Config.1		Config.2	
	Simulation	Experimental	Simulation	Experimental
SAPF with 2 LMs(n =7)	99.10%	98.74%	97.84%	96.84%
SAPF with 3 LMs(n =15)	98.79%	96.59%	97.28%	96.05%
SAPF with 4 LMs(n =31)	98.57%	96.06%	96.81%	94.87%

5. Conclusion

In this study, a single-phase asymmetric half-bridge cascaded multilevel inverter based series active power filter for harmonic voltage compensation is introduced. The SAPF is employed without a PPF since the purpose of this paper is to represent the level number effect on performance of the proposed inverter. A simple switching algorithm developed to obtain the required output voltage is also presented.

The SAPFs with levels of 7, 15 and 31 are simulated under two different loading conditions and experimental studies are carried out with a prototype developed.

The significant results of this study are summarized as follows:

- The multilevel inverter topology used in the proposed SAPF is the most advantageous topology depending on the number of switching devices to obtain the same output voltage level.
- The reduced number of switching devices, lower switching frequency and the absence of filter circuits significantly increase the system efficiency of the proposed SAPF. Thus, the system efficiency values in the range of 94.87% to 98.74% are achieved in the experimental studies.
- The easy acquisition of switching signals for the switching devices simplifies the structure of the control system.
- Experimentally obtained THD values of the load voltage confirm the simulation study. The measured THD values of the load voltage for six different conditions are in the range of 1.81% to 4.76% which are in compliance with the IEEE-519 Standard.

The results show that lower THD values can be obtained by increasing the level number of the inverter even under high harmonic distortion levels. With a level module, the level number can be easily increased, while the system efficiency is less influenced by the increase in the number of switching devices. Finally, it seems appropriate to use the asymmetric half-bridge cascaded multilevel inverter in SAPF applications even if two level modules are used.

Acknowledgements

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