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Individual DC Voltage Balancing Method at Zero Current Mode for Cascaded H-bridge Based Static Synchronous Compensator

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Abstract – Individual DC voltage balance problem is an inherent issue for cascaded H-bridge (CHB) based converter. When the CHB-based static synchronous compensator (STATCOM) is operating at zero current mode, the software-based individual DC voltage balancing control techniques may not work because of the infinitesimal output current. However, the different power losses of each cell would lead to the individual DC voltages unbalance. The uneven power losses on the local supplied cell-controllers (including the control circuit and drive circuit) would especially cause the divergence of individual DC voltages, due to their characteristic as constant power loads. To solve this problem, this paper proposes an adaptive voltage balancing module which is designed in the cell-controller board with small size and low cost circuits. It is controlled to make the power loss of the cell a constant resistance load, thus the DC voltages are balanced in zero current mode. Field test in a 10kV STATCOM confirms the performance of the proposed method.

Keywords: Static Synchronous Compensator (STATCOM), FACTS, High voltage power converters, Multilevel converter, Voltage Source Converter (VSC), DC voltage control

1. Introduction

Cascaded H-bridge (CHB) multilevel converter is the most popular topology for static synchronous compensator (STATCOM) in medium high voltage system, owing to its ability of achieving high voltage and high power with low rate switches. The Individual DC voltage balancing problem is an inherent issue of CHB-multilevel converter, and maintaining the DC voltages at a rated value is the fundament for a STATCOM to function properly [1-5]. When the STATCOM is operating at zero current mode (such as stand by status) , the main cause of individual DC voltage unbalance is the uneven power losses of different H-bridge cells, including the uneven losses in capacitors, absorption circuits, switching devices, diodes and drive circuits.

Many individual DC voltage balancing control strategies have been proposed and they can be divided into two categories. The first category is based on internal individual voltage controllers [5-11]. By detecting the output current, these methods regulate the fundamental output voltages respectively to control the fundamental energy exchange of each cell. The second category is the sorting method [12, 13], such as predictive sorting algorithm [14-16], distributed commutations modulation [17, 18]. These methods can realize DC voltage balance in the modulation progress by selectively distributing the PWM pulse (or carrier) to cells depending on the DC voltage rank list and the current detection.

However, these individual DC voltage balancing control methods may not work when a star-connected STATCOM is operating at the zero current mode. The zero current mode means the STATCOM has been started up and connected to the grid but the output current is nearly zero. This mode is frequent when the STATCOM is in debugging or stand by stage. The current is too low to be accurately extracted from the noise in zero current mode, so all these aforementioned individual DC voltage balancing methods may not function properly. In addition, delta-connected STATCOM may suffer less for this problem, because there can be a circling current within the delta-connected three phases without any grid power exchange, so aforementioned DC voltage balancing methods can still be utilized. But the circling current induced power loss will decrease the efficiency.

Ref. [19] has proposed a modified sorting algorithm to balance DC voltages in zero current mode by commutating the pulses in the middle of every switching periods. But the doubled switching frequency is the main drawback of this method, which greatly increases the power loss and imposes a heavy strain on the heat dissipation, especially in high voltage applications. Thus, the industrial methods to maintain DC voltage balance in zero current mode are mainly based on hardware, such as parallel resistors (or with an additional switch) on the DC bus . These hardware modules are designed to balance the power losses of each cell, thereby balancing the DC voltages. These methods are easy to be implemented, but the additional components induce some drawbacks on the cost, size and efficiency.

This paper focuses on the individual DC voltage balance

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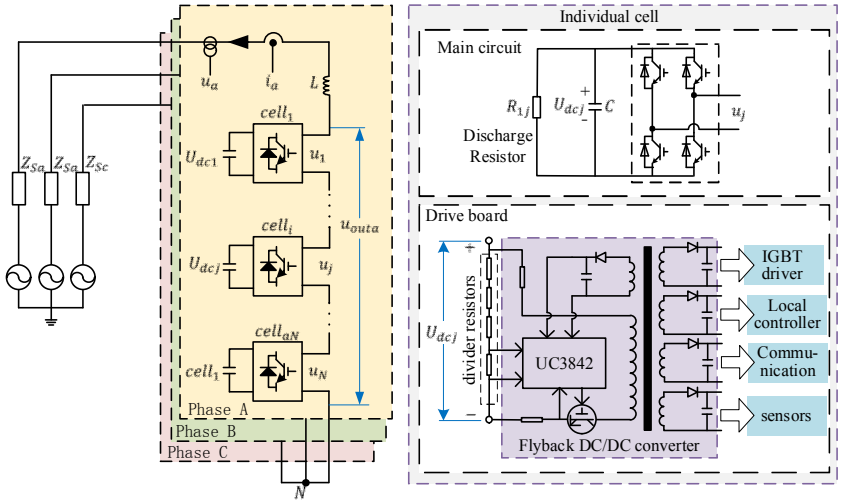


Fig. 1. Structure of star-connected STATCOM and individual H-bridge cell

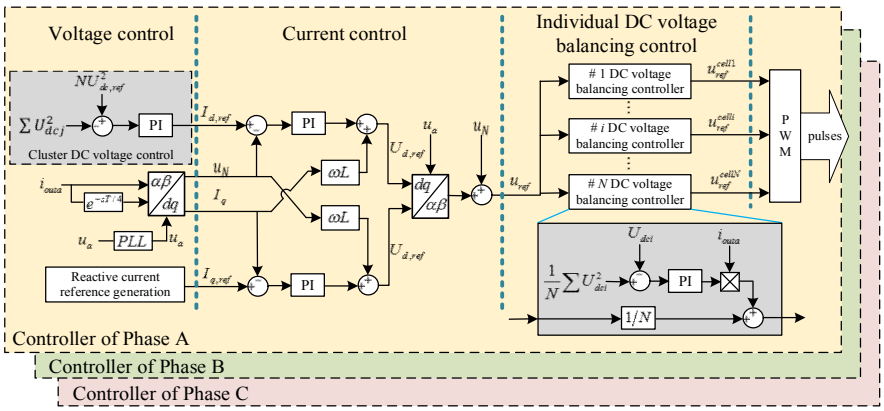


Fig. 2. CHB based STATCOM control system composed of three loops, i.e., cluster voltage control loop (outer loop), current control loop (inner loop) and individual DC voltage balancing loop

problem of a star-connected STATCOM (see Fig. 1) at zero current mode. Firstly, the power loss model of the STATCOM is built, and the traditional DC voltage balancing methods are briefly analyzed. Secondly, the reason of voltage unbalance in zero current mode is analyzed. Thirdly, based on the analysis, a small size and low cost module is designed in the cell-controller board to balance the DC voltages. A series of experiments are carried out to verify the validity of the method. At last, a comparison is carried out among 3 methods: the proposed controllable resistor on the cell-controller board, the parallel resistor on the DC bus and the controllable resistor on the DC bus. Which indicates that the proposed method is the most economical choice for the DC voltage balancing of the STATCOM at zero current mode.

2. Star Connected Statcom and its Control System

Fig. 1 shows the structures of a typical star-connected STATCOM and the individual H-bridge cell. Z_{sa}, Z_{sb}, Z_{sc} are the impedances of the grid; u_a, u_b, u_c are the sampled voltages of the point of common connection (PCC); i_{outa}, i_{outb}, i_{outc} are the sampled output currents of the STATCOM; L is the output filter of the STATCOM; u_{outa}, u_{outb}, u_{outc} are the overall voltages of the cascaded chains; N is the number of the H-bridge cells in a chain; u_1, $u_2 \cdots u_j \cdots u_N$ are the output voltages of each H-bridge cell; u_{dc1}, $u_{dc2} \cdots u_{dcj} \cdots u_{dcN}$ are the DC bus voltages of each H-bridge cell in a chain.

To implement the measurement, communication, control and gate drive of the four IGBTs, a local cell-controller is required in every cell and usually supplied by a 15V (or 24V) DC source. Due to the high voltage level of the CHB-based STATCOM, it is impossible to introduce the 15V DC sources from somewhere else into the H-bridge cell. Hence, all the cell-controllers are local supplied by the DC capacitor of the H-bridge with a small DC/DC converter (e.g. fly-back converter in Fig. 1).

Fig. 2 displays the overall control block diagram of CHB-based STATCOM. It is a dq-based multi-loop control

strategy, where the outer loop is designed to generate the d-axis and q-axis reference current, and the inner loop aims at controlling the output current to follow its reference. To obtain all the dq quantities, a Phase Lock Loop (PLL) is used to estimate the transformation angle θ of the grid voltage. Since the dq transformation is synchronized with the grid voltage, the d-axis and q-axis can be defined as active power axis and reactive power axis, respectively. Consequently, the d-axis reference current I_{d-ref} can be used to control the total capacitor voltages of each cluster; and the q-axis reference I_{q-ref} is a given reactive current output instruction, or it is generated by the controlling of the AC grid voltage.

The energy based cluster DC voltage control [2] is designed for compensating the STATCOM losses. The inner current control loop is a typical dq decoupling current controller based on PI regulators. It generates d-axis and q-axis reference voltage. By transforming them into abc coordinate system, the original modulation references of the three phases are obtained. Ideally, the original modulation reference should be simultaneously applied to all the H-bridge cells in one cluster.

To keep the STATCOM stable, the DC voltage balancing control is also necessary to compensate the uneven power loss of different cells. Usually, the power loss of the H-bridge cell can be modeled as in Fig. 3. It is divided into the series-loss and the parallel-loss. The series-loss is positively correlated to the AC current amplitude I and modeled as the current source $k_{loss}I$, including IGBT conduction losses, switching losses and output filter loss. The parallel-loss is positively correlated to the DC voltage and modeled as the resistor R_{lossj}, including the IGBT off-state losses, the capacitor loss, etc.

Based on the power loss model, the power flow in the H-bridge cell is derived as (1), where $R_j = R_{cj} // R_{lossj}$.

$$u_j(t)i(t) = U_{dcj}(t)C\frac{dU_{dcj}(t)}{dt} + \frac{U_{dcj}^2(t)}{R_j} + U_{dcj}(t)k_{loss}I \quad (1)$$

By ignoring the switching frequency ripples, the AC output voltage and current of the H-bridge cell are simplified into (2) and (3), where φ_j is the power angle of the AC output. Thus, (1) is simplified into (4).

$$u_j(t) = U_j \sin\omega t = M_j U_{dcj}(t)\sin\omega t \quad (2)$$

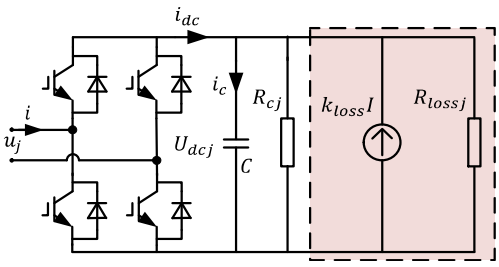


Fig. 3. Power loss model of the cell

$$i(t) = I\sin(\omega t + \varphi_j) \quad (3)$$

$$C\frac{dU_{dcj}(t)}{dt} = \frac{1}{2}M_j I[\cos\varphi_j - \cos(2\omega t + \varphi_j)] - \frac{U_{dcj}(t)}{R_j} - k_{loss}I \quad (4)$$

Since this paper concentrates on the long time DC voltage balancing issue of the CHB converter, the second harmonic power ripple can be ignored, hence, the power flow function is simplified into (5).

$$C\frac{dU_{dcj}(t)}{dt} = \frac{1}{2}M_j I\cos\varphi_j - \frac{U_{dcj}(t)}{R_j} - k_{loss}I \quad (5)$$

The left side of (5) represents the charge current of the DC capacitor, and the components on the right side of (5) represent the DC current provided by the AC side, the current of the parallel-loss, and the current of the series-loss.

In the steady state, (5) should equal 0 to keep the DC voltage stable. Under a symmetrical control and modulation method, the AC side power exchange of each cell is considered to be the same. On the other hand, the uneven power loss caused by the divergence of the components in different cells is unavoidable. It means that when the Eq. (5) of some cells equals 0, some others must not. This explains the reason for DC voltage unbalance.

Eq. (5) also shows the opportunities for DC voltage balancing methods. There are two parts in (5), $M_j cos\varphi_j$ and R_j, can be controlled to make (5) equal 0. Which signifies two different kinds of DC voltage balancing strategies: the AC side software-based DC voltage balancing strategy and the DC side hardware-based DC voltage balancing strategy.

There are different kinds of software-based DC voltage balancing methods [2-13] (including the one in Fig. 2), but, directly or indirectly, they all act up to the principle as shown in Fig. 4. According to the detected fundamental current phase and DC voltages, these methods change the AC side voltage of each cell to control the AC side power exchange.

However, when the AC side current is too low to be detected accurately from the noise, the output of these DC voltage balancing controllers would deviate. It makes the software-based DC voltage balancing controller invalid under zero current mode.

The hardware-based DC voltage balancing methods

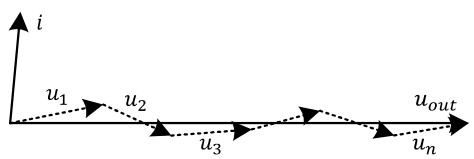


Fig. 4. Sketch of the software-based DC voltage balancing strategy

adjust the power loss resistor R_j by adding a shunt connected resistor or a switching resistor branch to the DC bus. These methods do not depend on the output current, so their function is not limited by the operating point of the STATCOM, and they can still work under zero current mode. But the hardware based methods have significant drawbacks on cost and size, due to the high voltage resistors and switches in the added branch. The purpose of this paper is to propose a novel low voltage hardware-based method to overcome these drawbacks.

3. DC Voltage Unbalance Analysis at Zero Current Mode

Because the output current is almost zero, the series-losses presented by the current source is negligible at the zero current mode. The parallel-loss represented by R_j includes two parts: the power loss on the main circuit components (including the power loss on the discharge resistor R_{cj}) and the power loss on the local cell-controller, which are modeled as resistor R_{j-main} and resisitor $R_{j-control}$, respectively. However, the power losses on the cell-controller board should be specially considered, because it is neither positively correlated to the output current nor the DC voltage. The power losses of the sensor, digital controller, communication model and the drive circuits are almost constant, so the local cell-controller board is nearly a constant power load. Hence, the resistor $R_{j-control}$ is a variable resistor.

Table 1. parameters of the tested H-bridge cell

Main circuit	
IGBT mode	FF450R17ME4
DC Capacitor value	4×600 uf
IGBT switching frequency	600 HZ
Rated AC voltage (RMS)	481V
Rated AC current (RMS)	247A
Rated DC voltage	840V
DC discharge resistor	50kΩ
cell-controller	
MOSFET of flyback	IRF640NS
Switching frequency of flyback	50 kHz
Local controller chip	CPLD 1270
IGBT drive chip	M57962AL

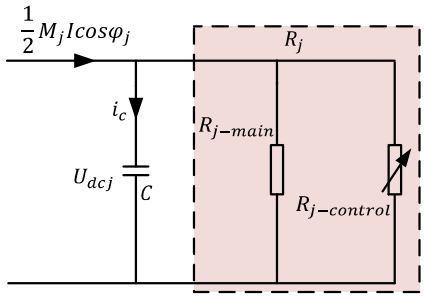


Fig. 5. Power loss model of the cell at zero current mode

According to (5) and ignoring the series-losses, the model of the H-bridge cell is changed into the one as in Fig. 5.

We carried out a series of experimental tests to measure the power losses of the whole cell and the cell-controller in zero current mode, respectively. At the same time, the power losses on the main circuit are calculated consequently. The parameters of the tested H-bridge cell are as shown in Table 1. The data of the test results are shown in Fig. 6.

Fig. 6 verified that the power loss on the main circuit is nearly in direct proportion to the DC voltage, while the power loss on the cell-controller board is almost a constant power load. And it also shows that the total power losses on an H-bridge at the zero current mode are about tens of watts.

By the data in Fig. 6, the equivalent resistances of these power losses can be easily calculated. The curves of R_{j-main}, $R_{j-control}$ and R_j versus DC voltage are presented in Fig. 7. They reveal that the main circuit is nearly a constant resistance load, while the cell-controller is nearly a constant power load. And the overall equivalent resistor R_j is positively correlated to the DC voltage.

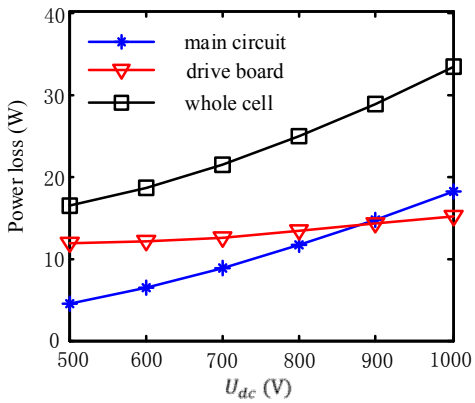


Fig. 6. Power losses under different DC voltages in zero current mode

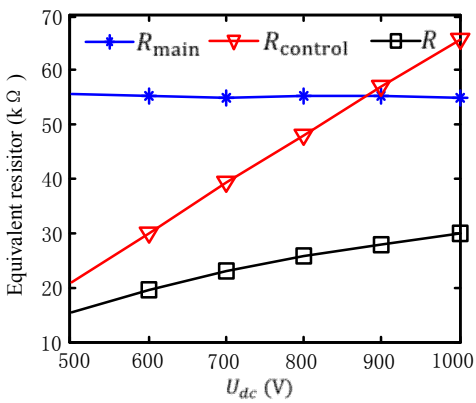


Fig. 7. Equivalent resistors under different DC voltages in zero current

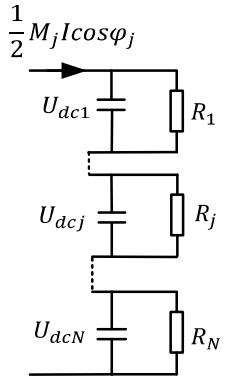


Fig. 8. Equivalent circuit of the cascaded chain at zero current mode

Because the current $\frac{1}{2} M_j I\cos\varphi_j$ are the same for all the cells in one CHB chain, we can connect the power loss model of each cell in series. Hence the equivalent circuit of the CHB chain is obtained as in Fig. 8.

By solving the Eq. (5), the expression of the DC voltage is obtained as (6). After a long time at zero current mode, the DC voltage is as (7).

$$U_{dcj}(t) = \frac{1}{2} M_j I \cos\varphi_j R_j - \frac{1}{2} e^{-t/CR_j} \tag{6}$$

$$U_{dcj} = \lim_{t\to\infty} U_{dcj}(t) = \frac{1}{2} M_j I \cos\varphi_j \cdot R_j \tag{7}$$

Thus, we have (8).

$$\frac{U_{dcj}}{R_j} = \frac{1}{2} M_j I \cos\varphi_j \tag{8}$$

According to the model in Fig. 8, we have (9).

$$\frac{U_{dc1}}{R_1} = \frac{U_{dc2}}{R_2} = \cdots = \frac{U_{dcj}}{R_j} = \cdots = \frac{U_{dcN}}{R_N} \tag{9}$$

It shows that the equivalent resistors R_j work as a voltage-sharing circuit. According to the voltage sharing principle (9), the ratios among DC voltages are the same with the ratios among the resisters.

If the cell-controller is not considered, R_j only involves $R_{j\text{–main}}$ which is a constant resistor. Thus the DC voltages will reach a stable state corresponding to (9). Because $R_{j\text{–main}}$ may vary from cell to cell, the stable value of the DC voltages may be different. However the difference will not be very big, which is acceptable in the zero current mode.

If the cell-controller is considered, influenced by the variable resistor $R_{j\text{–control}}$, the overall equivalent resistor R_j decreases with the decrement of the DC voltage, vice versa. Assuming the DC voltage of one cell is a little higher than others, the R_j would also be a little higher than that of others. Then, according to the voltage sharing principle (9), the DC voltage of the cell would become much higher, which would lead to a much higher R_j. Thus a positive feedback is constituted, resulting in the divergence of DC voltages. Although the power loss differences among the cells are small, when the STATCOM keeps operating at the zero current mode for a long time, this positive feedback loop would pose a high risk of crash on the system.

4. The DC Voltage Balancing Module in the Cell-Controller Board

Theoretically, we can choose an appropriate resistor to adjust the power loss of the cell to a unified value, thus the DC voltage can be balanced at the zero current mode. But the power losses of the cells would vary with time because the parameters of the components may change with temperature and many other factors during the life time of the STATCOM. The resistor chosen at first may mismatch the requirement of the loss balancing after a period of time. So, it is invalid to use different resistors to adjust the power loss of the cells. This problem is overcame by the adaptive load designed in this paper. Moreover, to use the same resistor and switch in all cells helps a lot for the manufacture processes.

The proposed DC voltage balancing module is essentially an adaptive load implemented by low voltage MOSFET and resistors in the cell-controller board as shown in Fig. 9. This module only works at zero current mode. The working principle of the module is adaptively increasing the power loss on the cell-controller when the DC voltage is higher than the average value. DC voltage of the cell U_{dci} is compared with the average DC voltage of the cluster $\frac{1}{N}\Sigma U_{dci}$. The difference of them is transferred into a duty rate D through a P (or PI) controller. The duty rate D is used to control the switch-on time of the MOSFET through a PWM modulator. If the U_{dci} is larger than the average, the MOSFET is turned on to increase the power loss on the cell. The parameters of the P (or PI) controller can be used to set the adjusting speed of the module. By

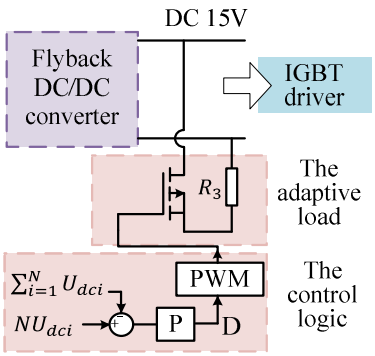


Fig. 9. The schematic of the module in the cell-controller board

this process, the overall equivalent resistance R is adaptively reduced to the average value, which results in balanced DC voltages.

Theoretically, the rated power of the voltage balancing module should be greater than the maximum deviation of the power losses on different cells.

The power loss of 12 H-bridge cells at zero current mode are measured under 840V DC voltage. Table 2 presents the results. It shows that the power loss deviation of these cells is 2.2W, which means the rated power of the adaptive load should be higher than 2.1 W.

Reasonably, higher rated power of the adaptive load means higher DC voltage balancing ability. However, the rated power of the adaptive load is limited by the power rate of the DC/DC supply on the local controller board.

The rated power of the fly-back converter in the local controller board is usually designed to be 20W-50W. But the adaptive load is connected to one of the output ports of the fly-back converter, so the rated power of the adaptive load should be limited lower. The parameters of the fly-back converter used in this paper are as shown in Table 3. In order to evaluate the impact of the adaptive load on the output of the fly-back converter, three different adaptive loads, 2.25 W, 7.5 W, and 12.5W, are implemented on the local controller board. By keeping the switch of the adaptive load on, the adaptive loads consumed the rated power. The results are recorded as in Fig. 10.

Fig. 10 shows that high rated power of the adaptive load module would distort the DC bus voltage of the IGBT driver, which puts the operation of the main circuit at risk. So the rated power of the adaptive load module should be designed as low as possible in the precondition of being larger than the power losses deviation of the H-bridge cells at zero current mode. Thus, we chose the 2.25W adaptive load module for the STATCOM in this paper.

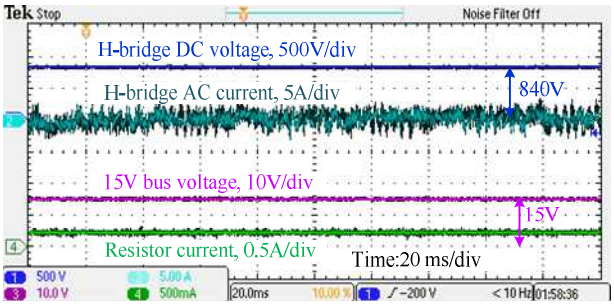
The layout of the 2.25W adaptive load module is as shown in Fig. 11. Because the close loop control based module do not highly depend on the precision of the resister, a normal 5% tolerance resister can be adopted. The control logic can also be easily realized in the local control chip of the cell-controller. The parameters are shown in table 2. The local CPLD sends out the switching signal, then through the amplification and isolation of a photo coupler, the switching signal is used to drive the MOSFET. Fig. 11 shows that the size of the proposed module is very small, and the Table 4 shows that its price is very low. These are two most important advantages of the proposed

Table 2. Power loss deviation at zero current mode

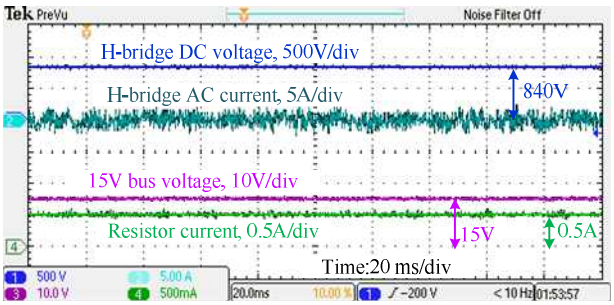
Cell #	Total loss	Controller loss	Cell #	Total loss	Controller loss
1	27.8	11.5	7	28.3	12.1
2	27.7	11.8	8	28.4	11.8
3	28.2	12.5	9	26.7	11.3
4	27.5	12.1	10	26.3	11.0
5	26.4	11.2	11	27.5	12.4
6	27.2	11.7	12	28.4	12.3

Table 3. Paramiters of the fly-back converter

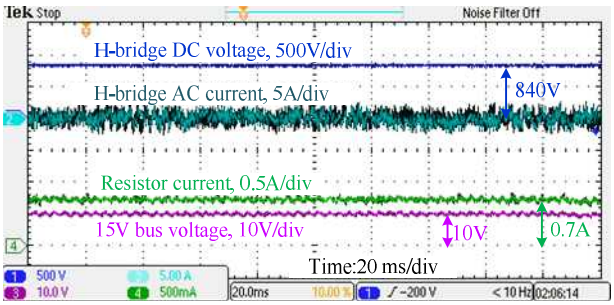
Item	Value
Controller chip	UC3842
MOSFET	2SK1317
Switching frequency	20 kHz
Rated power of the converter	40 W
Capacitor on the IGBT driver bus	1000 μF
Rated voltage of the IGBT driver bus	15 V



(a) 2.25W rated power



(b) 7.5W rated power



(c) 15W rated power

Fig. 10. Impact of the adaptive load with different rated powers on the Hbridge cell and its local supply converter in the controller board

Table 4. Parameters of the proposed module

Item	Value
MOSFET model	4N90C
MOSFET drive	photocoupler TLP421
Resister R_3	102Ω
MOSFET switching frequency	1 kHz
Rated power	2.25 W
Size	15×40 mm
Cost	$ 0.7

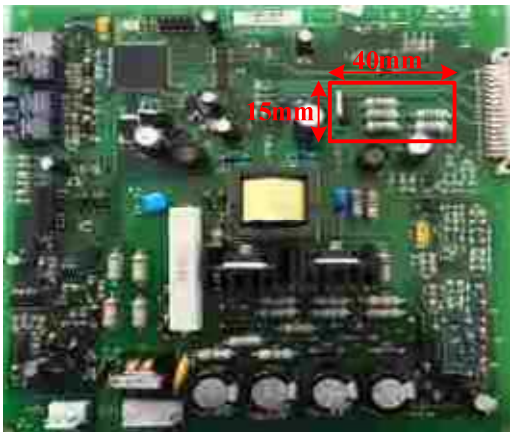


Fig. 11. The layout of the module in the cell-controller board

Fig. 12. 12-cell-cascaded 10 kV STATCOM

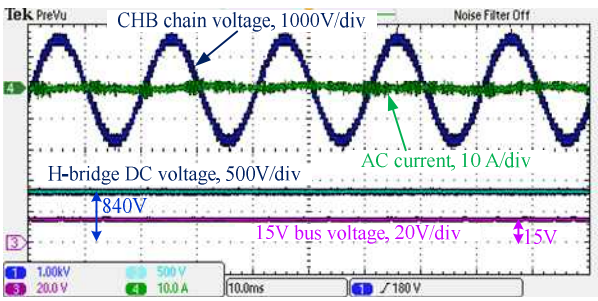


Fig. 13. Basic operating conditions of the STATCOM at zero current mode

method.

This adaptive load module has been verified in a 12-cell-cascaded 10 kV STATCOM product as shown in Fig. 12. The STATCOM was started up and connected to a 10 kV grid. Some measurements, including the CHB-chain voltage, the AC output current, the DC voltage of one H-bridge cell, and the voltage of 15 V bus in the cell, are presented in Fig. 13 to demonstrate the basic operating conditions at zero current mode. There was still a low amplitude AC current, but it was seriously distorted due to the switching harmonics and sensor noise.

At first, the DC voltage balancing module was deactivated. Since the differences among the power losses on cell-controllers are much smaller than the power level

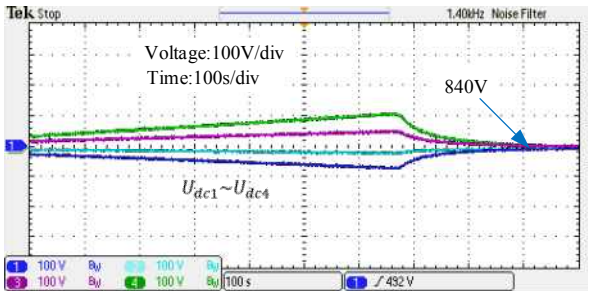


Fig. 14. DC voltage divergency and the effection of proposed module

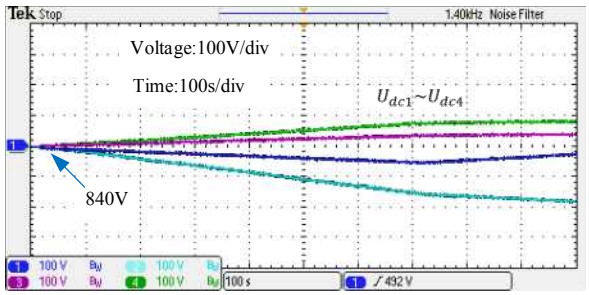


Fig. 15. DC voltgae divergency when the power loss deviation exceeds the ability of the adaptive load

of the DC capacitor, it cost a long time before the divergence of DC voltages becoming significant. Then the DC voltage balancing module was enabled, and the DC voltages were rebalanced in about 5 minutes. The experimental results are shown in Fig. 14.

In order to observe the phenomenon when the power deviation exceeds the rated power of the adaptive load module, we shunt connected a 100kΩ resistor to the DC bus of one cell. Therefore the power loss of this cell was increased and exceeded the range of the adaptive load module. By repeating the experiment processes, we got the results as in Fig. 15. When the adaptive load module was enabled, the DC voltage divergence of the changed cell was decelerated but not stopped, and the DC voltage balancing progresses of other cells were also influenced.

5. Comparison of Three Hardware Based Dc Voltage Balancing Schedules

To demonstrate the superiority of the novel method, a comparison is made among the proposed method and the other two hardware based methods. Besides the proposed module in the cell-controller board, the other two methods are a single resistor (as in Fig. 16(a)) and a branch composed of a resistor and a switch in series (as in Fig. 16(b)), which are installed on the DC bus.

A parallel resistor (as shown in Fig. 17) on the DC bus is a popular method. The mechanism is also the voltage sharing principle as shown in Fig. 8. Usually, a high

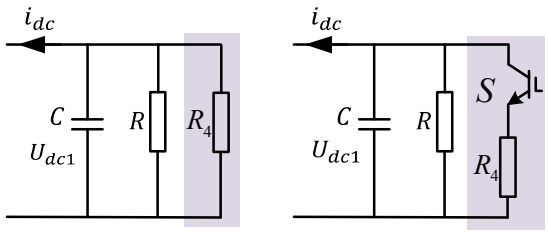


Fig. 16. Other two hardware based individual DC voltage balancing methods, i.e., (a) a single parallel resistor and (b) a parallel branch composed of a resistor and a switch in series

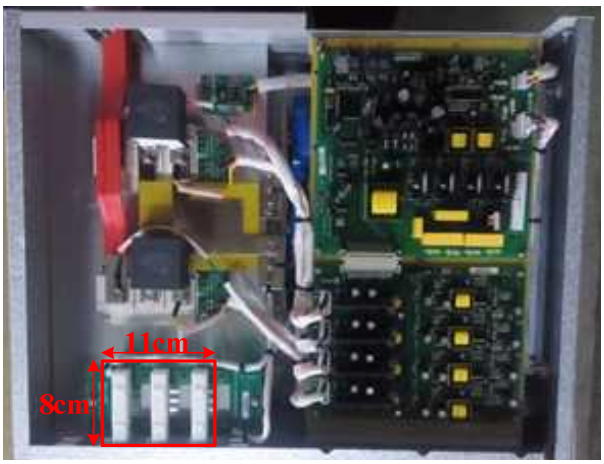


Fig. 17. H-bridge cell with a parallel resistor on the DC bus

precision resistors are used for the high accuracy of equal voltage sharing. Note the parallel of R and R_4 as R_{total}. Since the deviation of equivalent resistor R still exists, the additional parallel R_4 can only decrease the deviation of R_{total}, but not eliminate it. This non-ideal method will also cause the DC voltage divergence if the zero current mode lasts long enough. Moreover, for better balance of R_{total}, the value of R_4 should be chosen as small as possible, which poses a contradiction on power loss and DC voltage balance.

A parallel branch composed of a resistor and a switch in series is also a controllable load which can function as the proposed module. However, this branch has some advantages and disadvantages induced by the direct connection to the DC bus. The rated voltage of both the switch S and the resistor R_4 should be higher than the rated DC voltage. Compared with the module in the cell-controller board, to achieve the same DC voltage balancing power, the cost is higher and the size is bigger. On the other hand, the advantage of this branch is that it can be designed with higher rated power to enhance better power adjusting ability. However, the divergence of the power losses among the cells are only several watts at zero current mode, and the proposed module is enough for balancing them. Hence it is not necessary to design a high power hardware based DC voltage balancing branch.

Table 5. Comparison of the three hardware based methods

Methods	Advantages	Disadvantages
A single parallel resistor on DC bus (Fig. 16 (a))	Simple	High loss; Big size; No-ideal balancing.
A parallel branch on DC bus (Fig. 16 (b))	High power rate for DC voltage balancing; Ideal balancing.	High cost; Big size
A cell-controller boardbased module (Fig. 9)	Ideal balancing; Small size; Low cost.	Limited power rate for DC voltage balancing.

The comparative results of the three methods are concluded as in Table 3. It shows that the proposed DC voltage balancing module is the most economical method for DC voltage balance of STATCOM at the zero current mode.

6. Conclusions

In this paper, a novel method is proposed to guarantee the DC voltage balance of STATCOM at the zero current mode. Detailed analysis is provided for explaining the DC voltage unbalance mechanism in the CHB chain at zero current mode . The uneven power losses of the cells are the major cause of the individual DC voltage unbalance. Due to constant power load character of the drive board, the DC voltages would finally divergence in zero current mode. The typical DC voltage balancing control methods are restricted by the infinitesimal output current. A cell-controller board based DC voltage balancing module is proposed to adaptively adjust the power losses of each H-bridge cell. Compared with other DC voltage balancing modules which are directly connected to the DC bus, the proposed method is the most economical method. Experimental results are in good agreements with the theoretical analysis and have confirmed the effectiveness of the proposed method.

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