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Electrical Characteristics of SiC Lateral P-i-N Diodes Fabricated on SiC Semi-Insulating Substrate

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Abstract – Static characteristics of SiC (silicon carbide) lateral p-i-n diodes implemented on semi-insulating substrate without an epitaxial layer are investigated. On-axis SiC HPSI (high purity semi-insulating) and VDSI (vanadium doped semi-insulating) substrates are used to fabricate the lateral p-i-n diode. The space between anode and cathode (L_{AC}) is varied from 5 to 20 μm to investigate the effect of intrinsic-region length on static characteristics. Maximum breakdown voltages of HPSI and VDSI are 1117 and 841 V at L_{AC} = 20 μm, respectively. Due to the doped vanadium ions in VDSI substrate, diffusion length of carriers in the VDSI substrate is less than that of the HPSI substrate. A forward voltage drop of the diode implemented on VDSI substrate is 12 V at the forward current of 1 μA, which is higher than 2.5 V of the diode implemented on HPSI substrate.

Keywords: Silicon carbide, Semi-insulating, Lateral power device, High purity semi-insulating, Vnadium doped semi-insulating

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1. Introduction

Owing to its excellent physical and electrical properties, SiC (silicon carbide) is an important and attractive material for power device for high-temperature and high frequency applications [1-2]. Due to its material characteristics, SiC power device exhibits superior device characteristics compared to Silicon one such as high breakdown voltage, high temperature operation. However, in comparison with vertical SiC power devices, lateral SiC devices have been scarcely investigated. Demand for high-voltage lateral devices is high because of the necessity to implement both high-voltage device and low-voltage circuits on a single chip [3].

There have been reports describing static characteristics of 4H-SiC lateral device implemented on conducting substrate [4-5]. Although those devices show satisfactory characteristics, a thick lightly doped epitaxial layer is required to obtain high-breakdown voltage. Using semi-insulating substrate eliminates the need of the thick epitaxial layer [6]. It also offers an advantage of reducing the parasitic effects brought about by the electrical interference between adjacent devices in integrated circuits, such as conductive coupling between the devices through the substrate. Although 4H-SiC lateral device fabricated on semi-insulating substrate has been also reported, it also used additional p-type epitaxial layer grown on the semi-insulating substrate [7]. Due to the highly doped epitaxial layer, the lateral devices fabricated on the semi-insulating substrate showed higher leakage current at reverse bias condition.

In this paper, we investigated the static characteristics of 4H-SiC lateral device implemented on two types of SiC semi-insulating substrates, HPSI (high purity semi-insulating) and VDSI (vanadium doped semi-insulating) substrate. The purpose of this paper was to figure out the potential of SiC semi-insulating substrate as a candidate for fabricating the lateral devices without using the epitaxial layer. On-axis SiC HPSI and VDSI substrate were used to fabricate the lateral diodes, and breakdown and forward characteristics of the devices were investigated.

2. Device Structure and Fabrication

Fig. 1 shows the cross-sectional view and top-view of the lateral p-i-n diode implemented on HPSI and VDSI substrate without epitaxial layer. Device parameters used in fabrication are given in table 1. As shown in Fig. 1(b), the space between anode and cathode (L_{AC}) is varied from 5 to 20 μm and width of the device is 100 μm. Other design parameters are also shown in Fig. 1(b).

4H-SiC lateral p-i-n diodes are fabricated on the two types of on-axis semi-insulating substrate (HPSI and VDSI) in sequence of multi-step ion-implantation. Semi-insulating substrate is used as intrinsic layer without any growth of epitaxial layers. In order to obtain ohmic contacts, ion-implantation is performed with total ion dose of 2.81 × 10^{15}/cm^3 and 2.38×10^{15}/cm^3 at an elevorated temperature of 500°C for each anode (Al/P$^+$) and cathode (Nitrogen/N$^+$) regions, respectively. Because, the on-axis substrate were

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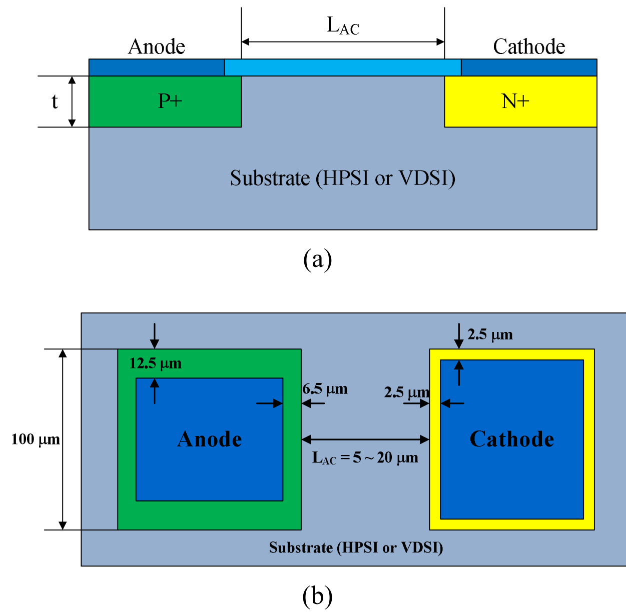

Fig. 1. (a) Cross-sectional view and (b) top-view of the lateral p-i-n diode

Table 1. Device parameters used in fabrication

Parameters	Doping Conc. ($/cm^3$)	Depth (µm)	Length (µm)
P+ anode	2.81×10^{15}	0.3	-
N+ cathode	2.38×10^{15}	0.3	-
Intrinsic layer	Semi-insulating	-	5 - 20

used to fabricate the diode, tilt angle of 4 degree was used to avoid the channelling effect during ion implantation. After ion implantation and high-temperature annealing for activation of ions, oxidation and No annealing were carried out to passivate the surface and suppress the surface recombination leakage current. Ohmic contact was formed by opening a passivation layer by reactive ion etching (RIE) and deposition of 30 nm-thick Ni. The devices were annealed at 950 °C for 90 s to form Ni_2Si silicide. Finally, Ti/Au pad metal was patterned on each anode and cathode.

3. Results and discussion

3-1. Simulation results

To verify the usability of semi-insulating substrate as possible material for devices, numerical simulations by using two-dimensional device simulator ATLAS [8] were performed. Basic device parameters used in the simulation are shown in Table 1. To investigate the effect of deep traps in the substrate, trap levels and density were taken into account by assuming an acceptor-like trap level and density of 0.67 eV, $2\times10^{13}/cm^3$ for HPSI and 1.03 eV, $1.75\times10^{17}/cm^3$ for VDSI substrate, respectively [9-11].

Fig. 2 shows simulated breakdown characteristics of

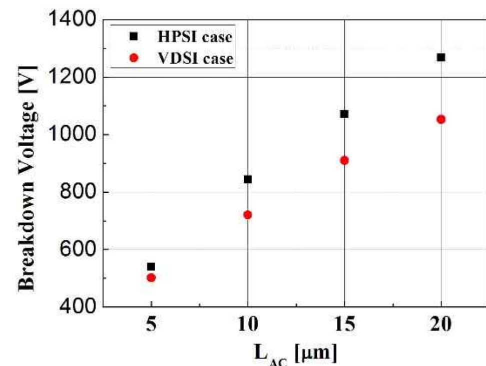

Fig. 2. Simulated breakdown voltages as a function of diode length (L_{AC})

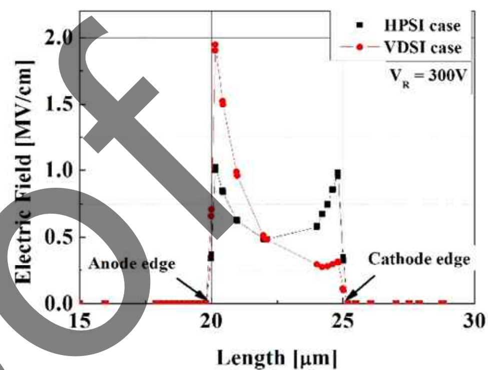

Fig. 3. Surface electric field distributions simulated at V_{anode} = -300 V

the lateral p-i-n diode implemented on HPSI and VDSI substrate when L_{AC} is varied from 5 to 20 µm. As shown in this figure, breakdown voltage of the lateral p-i-n diode on VDSI substrate is less than that on HPSI substrate, due to the different trap levels.

Surface electric field distribution simulated V_{anode} = -300 V shown in Fig 3. As shown in the figure, the anode side electric field for VDSI is higher than that for HPSI. This is the result of higher space charge density in the VDSI case, and the lower breakdown voltages of VDSI in Fig. 1 are also explained.

Breakdown characteristics of the lateral p-i-n diodes on HPSI and VDSI substrates were affected by deep traps in the substrate. Under avalanche breakdown conditions, due to the high electric field within intrinsic region of the lateral p-i-n diode, electrons (captured by acceptor-like traps) are swept out from the traps, leading to a change of the charge state of the traps. This kind of charge change increases the space charge density in the intrinsic region and results in a decrease of the breakdown voltage.

In case of VDSI substrate, due to the doped vanadium ions, the density of acceptor-like trap is higher than that of the HPSI substrate. In fact, vanadium in SiC is an amphoteric impurity. It acts as an acceptor-like trap in n-type SiC, and as a donor-like trap in p-type SiC. The VDSI

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substrate that we used to fabricate p-i-n diode is n-type, and doped vanadium ions are acting as acceptor-like traps. Therefore, increase of space charge density of the diode on VDSI substrate is larger than that of the diode on HPSI substrate.

Fig. 4 shows simulated forward characteristics of the lateral p-i-n diode on each substrate when LAC is 5 μm. As shown in the figure, forward voltage of the diode on VDSI substrate is higher than that of the diode on HPSI substrate. As mentioned above, acceptor trap density of the VDSI substrate is higher than that of the HPSI substrate.

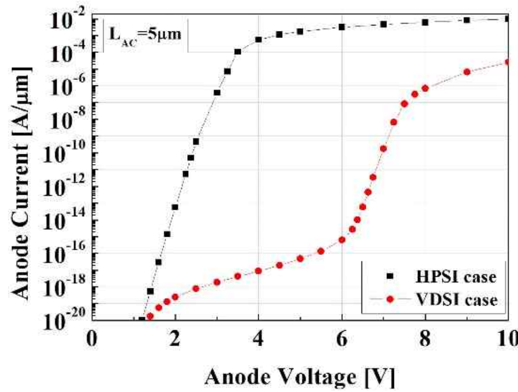
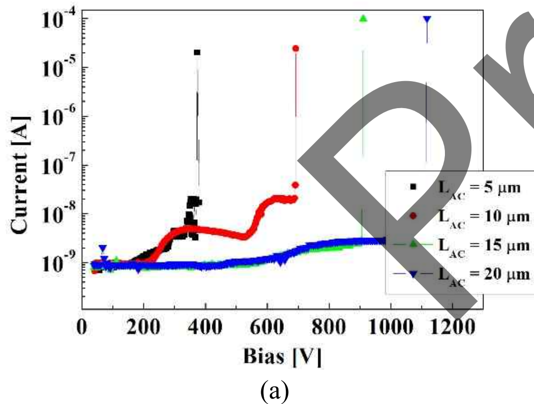
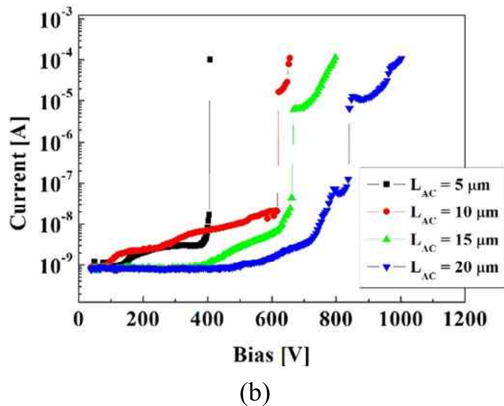


Fig. 4. Forward characteristics of the device simulation results



(a)



(b)

Fig. 5. Reverse I-V characteristics of lateral p-i-n diodes implemented on (a) HPSI and (b) VDSI substrate

Therefore, under forward bias condition, more electrons are captured by the traps in VDSI substrate and this will cause higher forward voltage of the diode.

3.2. Experimental results and discussion

All measurement in this paper were performed at room temperature. Fig. 5 shows reverse I-V curves of 4H-SiC lateral p-i-n diodes implemented on SiC HPSI and VDSI substrate as a function of L_{AC}. Device depicted in Fig. 1-(a) employs the RESURF (REduced SURface Field) concept [12].

To obtain RESURF structure, intrinsic layer of the p-i-n diode should be completely depleted before the field at the anode junction reaches the critical field for avalanche breakdown. And this requires $qN_DT < \varepsilon_S E_C$ where N_D is the doping concentration, T is thickness of intrinsic layer, and E_C is critical electric field for avalanche breakdown [13]. Because, semi-insulating substrate was used as an intrinsic layer of the p-i-n diode, doping concentration of the intrinsic layer is considerably low and it will be completely depleted before electric field at the anode junction reaches the critical field. Therefore, we can assume that lateral p-i-n diode implemented on semi-insulating substrate employs RESURF concept. It means that breakdown voltage of the lateral p-i-n diode implemented on semi-insulating substrate can be determined by L_{AC} and critical electric field, E_C.

Theoretical breakdown voltage (V_B) shown in Fig. 6 can be calculated with Eq. (1), where E_C is critical electric field [13]. Measured and simulated breakdown voltages of the device are shown in Fig. 6 for comparison.

$$V_B \approx E_C \times L_{AC} \tag{1}$$

Where V_B is breakdown voltage, E_C is critical electric field. Critical field can be obtained from Eq. (2) [14].

$$E_C(4H-SiC) = \frac{2.49\times10^6 V/cm}{1-0.25\log_{10}(N/(1\times10^{16}))} \tag{2}$$

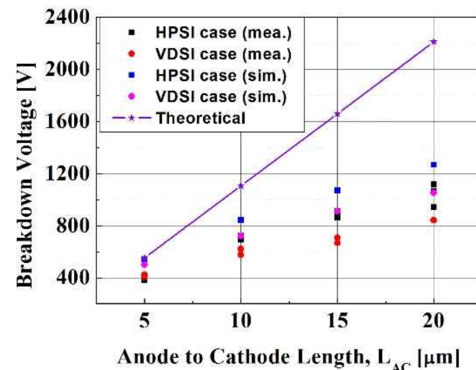


Fig. 6. Measured and simulated breakdown voltage as a function of L_{AC}

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We use N = 10^{11}/cm^3 for the calculation of the intrinsic region.

Fig. 6 shows measured breakdown voltages for the HPSI and VDSI substrates varies from 380-1117 V and 408-841 V as a function of LAC, respectively. In Eq. (1) and (2), trap parameters such as trap density or energy level are not included. Therefore, as shown in Fig. 6, measured breakdown voltage is less than the theoretical breakdown voltage due to the charge change effect caused by deep traps within semi-insulating substrate. Simulation results are closer to the measured results. Because we use only one kind of trap in device simulation while there are several kinds of deep traps exist in semi-insulating substrate, measured breakdown voltage is also lower than simulated breakdown voltage.

And also shown in the Fig. 6, breakdown voltage of the diode implementd on VDSI substrate is less than that of the diode implemented on HPSI substrate. As mentioned in previous section, breakdown characteristics of the semi-insulating substrate is affected by the deep traps within the intrinsic region. Therefore, due to the high trap density of the VDSI substrate, lateral p-i-n diode on VDSI substrate exhibit low breakdown voltage.

Fig. 7 shows forward I-V characteristics measured in the lateral p-i-n diodes implemented on HPSI and VDSI substrate. As shown in the figure, forward voltage of the diode implemented on HPSI and VDSI substrate is 2.5 and 12 V at I_A = 1μA when L_{AC} is 5 μm, respectively. In semi-insulating substrate, several kinds of traps such as $Z_{1/2}$, $EH_{6/7}$ are introduced during substrate growth process and they affect the diffusion length of the substrate [15]. Especially in VDSI substrate, due to the doped vanadium ions which are acting as acceptor-like traps, diffusion length of the carriers is shorter than that in HPSI substrate. Therefore, forward voltage of the diode implemented on VDSI substrate is much higher than that of the diode implemented on HPSI substrate.

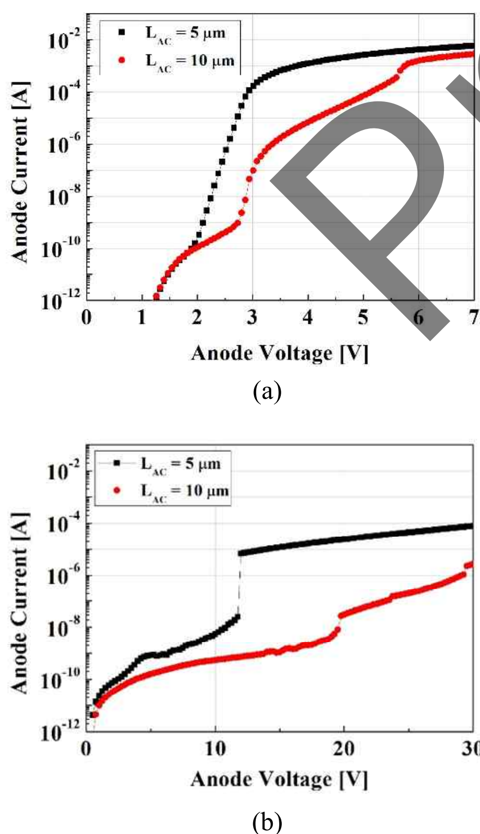

Fig. 7. Forward I-V characteristics of the device implemented on (a) HPSI and (b) VDSI

And as seen in the Fig. 7, due to the deep traps in semi-insulating substrate. sharp rise of currents were observed for both p-i-n diodes. In forward bias condition, some of the injected carriers are captured at traps. As applied voltage increases the injected carriers also increases and more traps are filled. The voltage where all the traps are filled is known as trap filled limited voltage and this voltage depends on the trap density [16]. After all the traps are filled then sharp in current occurs. As mentioned above, due to the doped vanadium ions, trap density of the VDSI substrate is higher than that of the HPSI substrate. And it makes trap filled limited voltage of the diode implemented on VDSI substrate is larger than that of the diode implemented on HPSI substrate.

Diode implemented on HPSI and VDSI substrate with L_{AC} = 5 μm has an active area of 0.05×10^{-4} cm^2 excluding pads. Each diodes exhibit 1 mA of forward operating current (I_F) at 3.8 V for HPSI case and 53.75 V for VDSI case respectively. On-resistance (R_{ON}) for both diode is 19.3 mΩcm^2 for HPSI and 270 mΩcm^2 for VDSI substrate when I_F = 1 mA, respectively. Figure of Merit (FOM, BV^2/R_{ON}) of diode on HPSI and VDSI substrate is 8.3 MW/cm^2 and 0.6 MW/cm^2 , respectively.

4. Conclusions

Static characteristics of the 4H-SiC p-i-n diode implemented on HPSI and VDSI without epitaxial layer is presented. The effects of substrate and deep traps on device performance have been investigated. Measured breakdown voltage of p-i-n diode implemented on HPSI and VDSI substrate is 1117 and 841 V when L_{AC} is 20 μm, respectively. Because the carrier concentration of the semi-insulating substrate is considerably low, substrate type does not degrade the breakdown characteristics significantly. However, acceptor-like trap density of VDSI substrate is higher than that of the HPSI substrate. Because of increase of space charge layer caused by deep traps, breakdown voltage of the diode implemented on VDSI substrate is less than that of the diode implemented on HPSI substrate. Forward characteristics of the p-i-n diode is affected by substrate type and deep trap density. Forward voltage drop of the p-i-n diode implemented on HPSI and VDSI substrate is 2.5 V and 12 V at I_A = 1 μA when L_{AC} is 5 μm,

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respectively. Doped vanadium ions are acting as acceptor-like traps and diffusion length of holes in the VDSI substrate is shorter than that of the HPSI substrate. Therefore, forward voltage drop of the p-i-n diode implemented on VDSI substrate is higher than that of the p-i-n diode implemented on HPSI substrate. FOM of the SiC diode on HPSI substrate without epitaxial layer is 8.3MW/cm^2. This result is promising for realizing SiC diode on HPSI substrate for IC applications such as built-in protection circuit of IC, ESD(electro-static discharge), TVS(transient voltage suppressor). However, due to the high density of deep traps within substrate, FOM of the SiC diode on VDSI substrate is 14 times higher than that of the HPSI substrate. Therefore, in order to use the VDSI substrate for IC applications, it is needed to compensate the deep traps in the substrate.

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References

[1] M. Bhatnagar and B. J. Baliga, “Comparison of 6H-SiC, 3C-SiC, and Si for power devices”, *IEEE Trans. ED*, vol. 40, no. 3, (1993), pp. 645-655.

[2] R. J. Trew, H. B. Yan, and P. M. Mock, “The potential of diamond and SiC electronic devices for microwave and millimeter-wave power applications”, *Proc. IEEE*, vol. 79, (1991), pp. 598-620.

[3] W. S. Lee, K. W. Chu, C. F. Huang, L. S. Lee, M, J. Tsai, K. Y. Lee and F. Zhao, “Design and Fabrication of 4H-SiC Lateral High-Voltage Devices on a Semi-Insulating Substrate”, *IEEE Trans. ED*, vol. 59, no. 3, (2012), pp. 754-760.

[4] M. Noborio, J. Suda, and T. Kimoto, “4H-SiC lateral double RESURF MOSFETs with low on resistance” *IEEE Trans. ED*, vol. 54, no. 5, (2007), pp. 1216-1223.

[5] Y. Zhang, K. Sheng, M. Su, J. Zhao, P. Alexandrov, and L. Fursin, “1000 V 9.1 mΩcm2 normally off 4H-SiC lateral RESURF JFET for power integrated circuit applications” *IEEE EDL*, vol. 28, no. 5, (2008), pp. 404-407.

[6] C. F. Huang, J. R. Kuo, and C. C. Tsai, “High Voltage (3130V) 4H-SiC Lateral p-n Diodes on a Semi insulating Substrate”, *IEEE EDL*, vol. 29, no. 1, (2008), pp. 83-85.

[7] W. S. Lee, C. W. Lin, M. H. Yang, C. F. Huang, J. Gong and Z. Feng, “Demonstration of 3500-V 4H-SiC Lateral MOSFETs”, *IEEE EDL*, vol. 32, no. 3. (2011), pp. 360-362.

[8] Silvaco TCAD, ATLAS, Silvaco International Co. USA

[9] W. C. Mitchel, W. D. Mitchell, G. Landis, H. E. Smith, W. Lee and M. E. Zvanut, “Vanadium donor and acceptor levels in semi-insulating 4H- and 6H-SiC”, *J. Appl. Phys*., 101, (2007), 013707.

[10] W. C. Mitchel and W. D. Mitchell, “Compensation mechanism in high purity semi-insulating 4H-SiC”, *J. Appl. Phys*., 101, (2007), 053716.

[11] T. Dalibor, G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schoner, and N. Nordell, “Deep Defect Centers in Silicon Carbide Monitored with Deep Level Transient Spectroscopy”, *Phys. Stat. Sol*. (a), 162, (1997), pp. 199-225.

[12] J. A. Appels and H. M. J. Vaes, “High voltage thin layer devices (RESURF DEVICES),” *IEEE IEDM Tech. Dig*., (1979), pp. 238-241.

[13] T. Kimoto, J. A. Cooper, “Fundamentals of silicon carbide technology”, Wiley & Sons, Singapore, 2014, chap. 10 and app. C.

[14] A. O. Konstantinov, Q. Wahab, N. Nordell and U. Lindefelt, “Ionization rate and critical fields in 4H silicon carbide”, *Appl. Phys. Lett*., vol. 71, no. 1, (1997), pp. 90- 92.

[15] M. V. S. Chandrashekhar, I. Chowdhury, P. Kaminski, R. Kozlowski, P. B. Klein, and T. Sudarshan, “High Purity Semi-Insulating 4H-SiC Epitaxial Layers by Defect-Competition Epitaxy: Controlling Si Vacancies”, *Appl. Phys. Express*, vol. 5, (2012), 025502.

[16] A. Jain, P. Jumar, S. C. Jain, and V. Kumar, R. Kaur, R. M. Mehra, “Trap filled limit voltage (VTFL) and V2 law in space charge limited currents,” *J. Appl. Phys*., 102, (2007). 094505.

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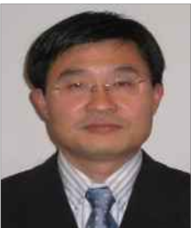

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