J Electr Eng Technol.2017; 12(?): 1921-718
http://doi.org/10.???/JEET.2017.12.3.1921

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Compact Current Model of Single-Gate/Double-Gate Tunneling Field-Effect Transistors

Yun Seop Yu† and Faraz Najam*

Abstract – A compact current model applicable to both single-gate (SG) and double-gate (DG) tunneling field-effect transistors (TFETs) is presented. The model is based on Kane's band-to-band tunneling (BTBT) model. In this model, the well-known and previously-reported quasi-2-D solution of Poisson's equation is used for the surface potential and length of the tunneling path in the tunneling region. An analytical tunneling current expression is derived from expressions of derivatives of local electric field and surface potential with respect to tunneling direction. The previously reported correction factor with three fitting parameters, compensating for superlinear onset and saturation current with drain voltage, is used. Simulation results of the proposed TFET model are compared with those from a technology computer-aided-design (TCAD) simulator, and good agreement in all operational bias is demonstrated. The proposed SG/DG-TFET model is developed with Verilog-A for circuit simulation. A TFET inverter is simulated with the Verilog-A SG/DG-TFET model in the circuit simulator; the model exhibits typical inverter characteristics, thereby confirming its effectiveness.

Keywords: Compact model, Band-to-band tunneling (BTBT), Surface potential, Tunneling field-effect-transistor (TFET)

1. Introduction

Tunneling field-effect transistors (TFETs) have recently attracted considerable attention as a potential solution to the increasing power density problem in complementary metal-oxide-semiconductor (CMOS) technology, which is limited by the 60 mv/dec subthreshold swing of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) at room temperature because of the thermionic emission of carriers injected from the source to the channel region [1,2]. Complementary TFETs (C-TFETs) in a standard 12-inch CMOS foundry have been recently demonstrated [3], and novel TFET-based circuits have been studied [4,5]. In order to efficiently design and simulate circuits consisting of TFETs or MOSFETs, an accurate and physics-based compact model for TFETs is needed.

There have been extensive studies of compact modeling of TFETs [6-13]. In some of the TFET models, the current is calculated by numerically integrating the band-to-band tunneling (BTBT) generation rate of tunneling carriers over the volume of the device [6]. A look-up table-based or behavioral model [7] of TFETs was reported; however, it is not a physics-based TFET model. A universal analytic model, based on the Kane-Sze formula for tunneling current and the smoothing function for saturation and superlinear onset of drain bias, has been developed, but it includes several fitting parameters [8]. Most of the compact models calculate the tunneling current by integrating the Kane's BTBT model [14] over one tunneling direction by assuming that the tunneling rate changes only in one direction and it is uniform in other directions [9-12]. In [9], the tunneling current is calculated by assuming that the electron generation rate follows the spatial distribution function. In [10], when the tunneling generation rate is integrated over one tunneling direction, a local electric field obtained from the quasi-2-D solution of Poisson's equation is considered. However, the current derived from the Kane's model has a critical problem that drain–source current is nonzero at zero drain–source bias, and the saturation and superlinear onset by drain–source bias are not included; thus, most TFET compact models use an empirical function [8-10] in order to compensate for these effects. In [13], an analytical model of the surface potential for both depletion as well as accumulation regimes is presented and the prediction of zero drain current at zero drain bias is physically modeled; however, at a high drain bias (over 1 V), the drain current has some error with no constant current.

In this paper, a compact current model applicable to both single-gate (SG) and double-gate (DG) TFETs is introduced. The model is based on the Kane's BTBT generation model. A new tunneling current expression developed using the derivatives of local electric field and potential with respect to the tunneling direction is proposed in Section II. Next, in order to investigate the validity of the proposed model, simulation results of the proposed model are verified with those of a technology computer-

† Corresponding Author: Dept. of Electrical, Electronic and Control Electronic Engineering and IITC, Hankyong National University, Korea. (ysyu@hknu.ac.kr)
* Dept. of Electrical, Electronic and Control Electronic Engineering and IITC, Hankyong National University, Korea. (faraznajam@hknu.ac.kr)
Received: January 20, 2016; Accepted: November 4, 2017

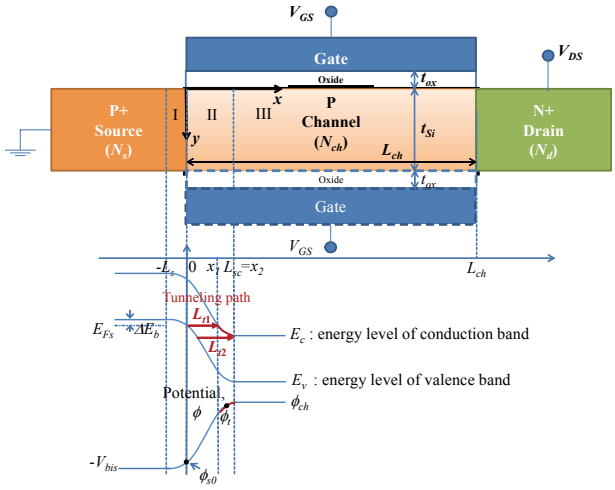

Fig. 1. Cross-sectional schematics of an SG/DG TFET structure. This figure shows an n-type TFET. In p-type TFET; the source and drain regions are n^+-Si and p^+-Si, respectively

Table 1. Device dimensions and electrical parameters

Symbols	DESCRIPTION	Unit
L_{ch}	Channel length	cm
W_{ch}	Channel width	cm
t_{si}	Silicon channel thickness	cm
T_{sieff}	Effective silicon channel thickness	cm
t_{ox}	Gate oxide thickness	cm
N_s	Source doping concentration	cm^{-3}
N_{seff}	Effective source doping concentration	cm^{-3}
N_d	Drain doping concentration	cm^{-3}
N_{ch}	Channel doping concentration	cm^{-3}
N_{tran}	Inversion charge density at transition in channel	cm^{-3}
ε_{ox}	Dielectric permittivity	-
ε_{si}	Channel permittivity	-
λ_{ch}	Characteristics length	cm
V_{FB}	Flat-band voltage	V
V_{GS}	Gate-source voltage	V
V'_{GS}	Effective gate-source voltage, $V'_{GS}= V_{GS} - V_{FB} - qN_{ch}\lambda^2_{ch}/\varepsilon_{si}$	V
V_{DS}	Drain-source voltage	V
I_{DS}	Drain-source current	A
$V_{bi,s}$	Source built-in voltage	V
ϕ_{ch}	Surface potential in the channel [12]	V
ϕ_0	$\phi_0 = qN_{seff}\lambda^2_{ch}/\varepsilon_{si}$	V
E_g	Energy bandgap	eV
ΔE_b	Difference between the energy levels of valance band E_v and electron quasi-Fermi E_{Fs} of the source	eV
E_{avg}	Average electric field	V/cm
A_k	Tunneling process parameter	$cm^{-1/2}V^{-5/2}s^{-1}$
B_k	Tunneling process parameter	V/cm
D	Tunneling process parameter distinguishing the direct (D=2) from the indirect (D=2.5). D=2.5 at Si.	-
Γ	Saturation shape fitting parameter [8] in (15)	V
λ	Saturation voltage fitting parameter [8] in (15)	V
V_{off}	Fitting parameter for minimum V_{GS} to describe both superlinear onset and saturation current [8] in (15)	V

aided-design (TCAD) simulator in Section III. Finally, Section IV concludes this paper.

2. Model Development

Fig. 1 shows the cross-sectional schematics of a SG/DG-TFET structure. A TFET consists of a source (S), channel, drain (D), gate oxide, and single/double-gates (SG/DGs). In Fig. 1, the SG-TFET structure can be obtained by replacing both the oxide and gate below the channel with a thick oxide layer. Table 1 shows the device dimensions and electrical parameters. The surface potential of the source-channel region at an arbitrary bias condition is shown in the bottom of Fig. 1. In this study, the surface potential is modeled using the quasi-2-D solution [12] of Poisson's equation. The length of tunneling path L_t for the entire range of the energy window can be calculated from the surface potential ϕ_t at tunneling end-point x, which is shown in Table 2.

Using the Kane BTBT generation model in which the carriers tunnel from the valence band of the source to the conduction band of the channel, the drain current can be calculated by integrating the generation rate over the volume of the tunneling window as given by [14, 15]

$$I_{DS} = q\int A_k E^D \exp\left(-B_k/E\right)dV. \quad (7)$$

Under the assumption that the tunneling current is uniform across the channel width W_{ch} and effective channel thickness T_{sieff}, which is approximately valid for DG TFETs with thin body thickness and SG-TFETs with maximum depleted thickness, a closed-form solution of the integral in (7) is given by

Table 2. Equations for length of tunneling path [9],[12]

Description, Symbols	Equations
Length of tunneling path, L_t	$L_t = L_s + L_{sc} - \lambda_{ch}\cosh^{-1}\left(\frac{V'_{GS}-\phi_t}{V'_{GS}-\phi_{ch}}\right) - \sqrt{\frac{2\varepsilon_{si}}{qN_{seff}}\left(\pm\phi_t + V_{bi,s} - \frac{E_g+\Delta E_b}{q}\right)}$ (1)
Surface potential at tunneling end-point x (in Region II), ϕ_t	$\phi_t = V'_{GS} - (V'_{GS}-\phi_{ch})\cosh\left(\frac{x-L_{sc}}{\lambda_{ch}}\right)$ (2)
Depletion width in source region, L_s	$L_s = \sqrt{\frac{2\varepsilon_{si}(\pm\phi_{s0}+V_{bi,s})}{qN_{seff}}}$ (3)
Depletion width in channel region at source side, L_{sc}	$L_{sc} = \lambda_{ch}\cosh^{-1}\left(\frac{V'_{GS}-\phi_{s0}}{V'_{GS}-\phi_{ch}}\right)$ (4)
Surface potential at source junction, ϕ_{s0}	$\phi_{s0} = V'_{GS} \pm \phi_0 \mp\sqrt{(V'_{GS}-\phi_{ch})^2+\phi_0^2+2\phi_0(\pm V'_{GS}+V_{bi,s})}$ (5)
Shortest tunneling surface potential, $\phi_{t,min}$	$\phi_{t,\min} = V'_{GS} \pm \phi_0 \mp\sqrt{(V'_{GS}-\phi_{ch})^2+\phi_0^2+2\phi_0\left(\pm V'_{GS}+V_{bi,s}-\frac{E_g+\Delta E_b}{q}\right)}$ (6)

In (1), (3), (5) and (6), the plus and minus signs are used for n-type and p-type TFETs, respectively.

$$I_{DS} = qA_k W_{ch} T_{sieff} \int_{x_1}^{x_2} E^D \exp\left(-B_k / E\right) dx. \quad (8)$$

At $x = x_1$, the difference between the source conduction band and channel conduction band is $E_g + \Delta E_b$, and at $x = x_2$, the difference between the source conduction band and channel conduction band reaches $E_g + \Delta\varphi$, where $\Delta\varphi$ is the difference between source valance band and channel valance band.

By the combination of the derivatives of the surface potential at tunneling end point x in Region II, as shown by (2), with respect to x and (2), the following equation is derived:

$$d\phi_t = \frac{\lambda_{ch}^2 E dE}{\sqrt{\left(V'_{GS} - \phi_{ch}\right)^2 + \lambda_{ch}^2 E^2}}, \quad (9)$$

where E is the local electric field in the x-direction. Eq. (9) is arranged as

$$\frac{dE}{dx} = -\frac{\sqrt{\left(V'_{GS} - \phi_{ch}\right)^2 + \lambda_{ch}^2 E^2}}{\lambda_{ch}^2}. \quad (10)$$

When (10) is applied to (8), we obtain

$$I_{DS} = -\lambda_{ch}{}^2 q A_k W_{ch} T_{sieff} \int_{E_1}^{E_2} dE \frac{E^D \exp\left(-B_k / E\right)}{\sqrt{\left(V'_{GS} - \varphi_{ch}\right)^2 + \lambda_{ch}^2 E^2}}, \quad (11)$$

The electric field across the tunnel junction can be approximately used as the average electric field, $E \approx E_{avg} = E_g/qL_t$ [10-13], and applying $dE \approx -dL_t(E_g/qL_t^2)$ to (11) yields

$$I_{DS} = qA_k W_{ch} T_{sieff} \lambda_{ch}^2 \left(\frac{E_g}{q}\right)^{D+1} \int_{L_{t,\min}}^{L_{t,\max}} dL_t \frac{L_t^{-D-2} \exp\left(-qB_k L_t / E_g\right)}{\sqrt{\left(V'_{GS} - \phi_{ch}\right)^2 + \frac{\lambda_{ch}^2 E_g^2}{q^2 L_t^2}}}, \quad (12)$$

where $L_{t,min}$ and $L_{t,max}$ denote the minimum and maximum length of the tunneling path in the depletion region, respectively. $\phi_{t,min}$ can be calculated from (6) in Table 2 when $\partial L_t/\partial \phi_t = 0$, and then, $L_{t,min}$ can be obtained by applying $\phi_{t,min}$ to (1). $L_{t,max}$ corresponds to the lower limit of the tunnel energy window where ϕ_t reaches the value of ϕ_{ch}, as shown in the energy band diagram of Fig. 1.

If we assume that the variation of polynomial terms in the interval from $L_{t,\min}$ to $L_{t,max}$ in the integral part of (12) is negligible compared with that of the exponential term [10,13,15], (12) is reduced to the following analytical formula:

$$I_{DS} = \pm \frac{qA_k W_{ch} T_{sieff} \lambda_{ch}^2}{B_k} \left(\frac{E_g}{q}\right)^{D+2} \left[S\left(L_{t,\min}\right) - S\left(L_{t,\max}\right)\right], \quad (13)$$

where $S(L_t)$ is defined as

$$S\left(L_t\right) = \frac{L_t^{-D-2} \exp\left(-qB_k L_t / E_g\right)}{\sqrt{\left(V'_{GS} - \phi_{ch}\right)^2 + \frac{\lambda_{ch}^2 E_g^2}{q^2 L_t^2}}}. \quad (14)$$

The plus and minus signs in (13) are used for n-type and p-type TFETs, respectively.

The effects of superlinear onset, which arise from the Fermi occupancy of filled states in the source and unoccupied states in the channel, and the saturation of I_{DS} with V_{DS} are neglected. The following correction factor f [8] is thus needed to compensate for superlinear onset and saturation current with V_{DS}:

$$f = \frac{1 - \exp\left(-\frac{V_{DS}}{\Gamma}\right)}{1 + \exp\left(\frac{\lambda \tanh\left(V_{GS} - V_{off}\right) - V_{DS}}{\Gamma}\right)}. \quad (15)$$

For SmartSpice [16] circuit simulations with the proposed SG/DG-TFET model, we developed its Verilog-A model.

3. Model Validation

In order to show the validity of our proposed model, the TCAD simulation in ATLAS [17] is used. The nonlocal BTBT, Shockley-Read-Hall recombination, Lombardi mobility, auger recombination, and bandgap-narrowing model were used in TCAD for the transport behavior of the SG/DG TFETs under consideration. Three types of TFET are fitted in order to show that the proposed model is valid for SG and DG-TFETs with different silicon body thicknesses, silicon effective tunneling masses, gate oxide thicknesses, and gate oxide materials. Two of the types are n-type and p-type SG-TFETs with silicon body, silicon effective tunneling mass $m_h = 0.34m_o$ (where m_o is the electron rest mass) for holes and $m_e = 0.2m_o$ for electrons, high-k gate oxide (HfO_2), t_{si} =20 nm, t_{ox} = 3 nm, and L_{ch} = 50 nm, and the other is an n-type DG-TFET with silicon body, silicon effective tunneling mass $m_h = 0.49m_o$ and $m_e = 0.19m_o$, gate oxide (SiO_2), t_{si} = 10 nm, t_{ox} = 2 nm, and L_{ch} = 50 nm. The doping concentrations of both SG and DG-TFETs are $N_s = 10^{20}$ cm^{-3}, $N_{ch} = 10^{12}$ cm^{-3}, and $N_d = 5\times10^{18}$ cm^{-3}.

Fig. 2 shows the surface potential profiles of an n-type SG-TFET and an n-type DG-TFET in the source–channel region as a function of the gate–source voltage. The

simulation results of the analytical potential model (lines) [12] are in good agreement with the TCAD simulation results (symbols) for both n-type SG and DG-TFETs. The fitted parameters are N_{seff} =1.5×10^{19} cm^{-3} and N_{tran} = 1.0×10^{18} cm^{-3} for the SG-TFET, and N_{seff} = 4.4×10^{19} cm^{-3} and N_{tran} = 2.0×10^{17} cm^{-3} for the n-type DG-TFET.

Using the parameters of n-type SG and DG-TFETs extracted in Fig. 2, Figs. 3(a) and (b) show the drain current-gate voltage (I_{DS}–V_{GS}) characteristics of the n-type SG and DG-TFETs for different drain-source voltages, respectively. The log and linear plots of I_{DS}–V_{GS} characteristics are shown in the left and right axes, respectively, in Fig. 3. The simulation results of the analytical model (lines) are in good agreement with the TCAD simulation results (symbols) for both n-type SG and DG-TFETs. The fitted parameters are A_k = 1.57×10^{20} cm$^{-1/2}$ V$^{-5/2}$s^{-1}, B_k = 2.29×10^7 V/cm, Γ = 0.075 V, λ = 0.6 V, and V_{off} = 0 V for the n-type SG-TFET, and A_k = 1.4×10^{19} cm$^{-1/2}$V$^{-5/2}$s^{-1}, B_k = 2.35×10^7 V/cm, Γ = 0.3 V, λ = 0.6 V, and V_{off} = 0 V for the n-type DG-TFET. A_ks and B_ks fitted in Figs. 3(a) and (b) are not equal because different tunneling masses for n-type SG and DG-TFETs are used in the TCAD simulation.

Using the parameters of n-type SG and DG-FETs extracted in Figs. 2 and 3, Figs. 4(a) and (b) show the drain current–drain voltage (I_{DS}–V_{DS}) characteristics of the n-type SG and DG-TFETs, respectively, for different gate–source voltages. The log and linear plots of I_{DS}–V_{GS} characteristics are shown in the left and right axes, respectively, in Fig. 4. The simulation results of the analytical model (lines) are in good agreement with the TCAD simulation results (symbols) for both n-type SG and DG-TFETs. Each A_k and B_k in Figs. 3 and 4 are constant with only tunneling material dependence [9-15], and do not have any dependence on drain and gate bias [18, 19].

Figs. 5(a) and (b) show I_{DS}–V_{GS} characteristics for different values of V_{DS}, and I_{DS}–V_{DS} characteristics for different values of V_{GS}, respectively, of the p-type SG-TFET. For simplicity, the device parameters of the p-type SG-TFET are same as those used for the n-type SG-TFET, except that the source and drain regions are doped with n and p-types, respectively, and the gate material is p$^+$-poly silicon. The log and linear plots are shown in the left and right axes, respectively, in Fig. 5. The simulation results of the analytical model (lines) are in good agreement with the TCAD simulation results (symbols) of the p-type SG-TFET. The fitted parameters are N_{seff} = 1.4×10^{19} cm^{-3}, A_k = 4.9×10^{19} cm$^{-1/2}$V$^{-5/2}$s^{-1}, B_k = 2×10^7 V/cm, Γ = 0.095 V, λ = 0.6 V, and V_{off} = 0 V.

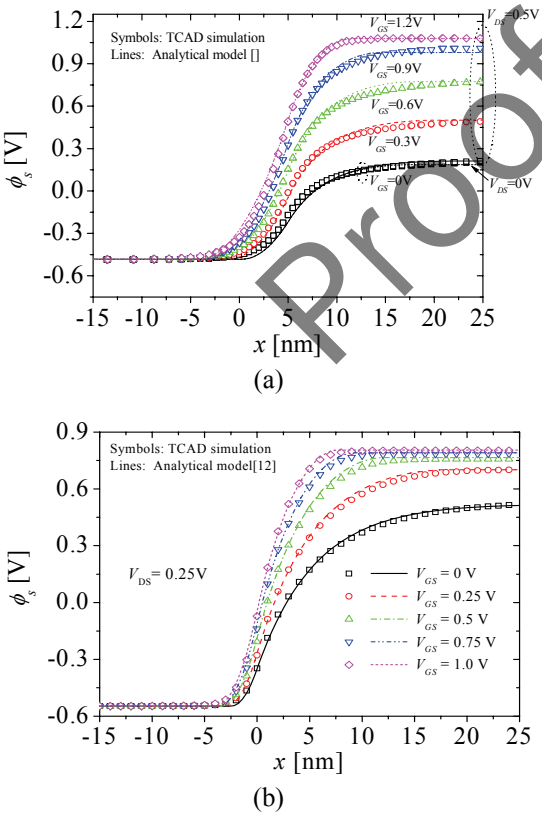

Fig. 2. Surface potential profiles of (a) an SG-TFET at V_{DS} = 0 and 0.5 V, and (b) a DG-TFET at V_{DS} = 0.25 V, as a function of V_{GS}

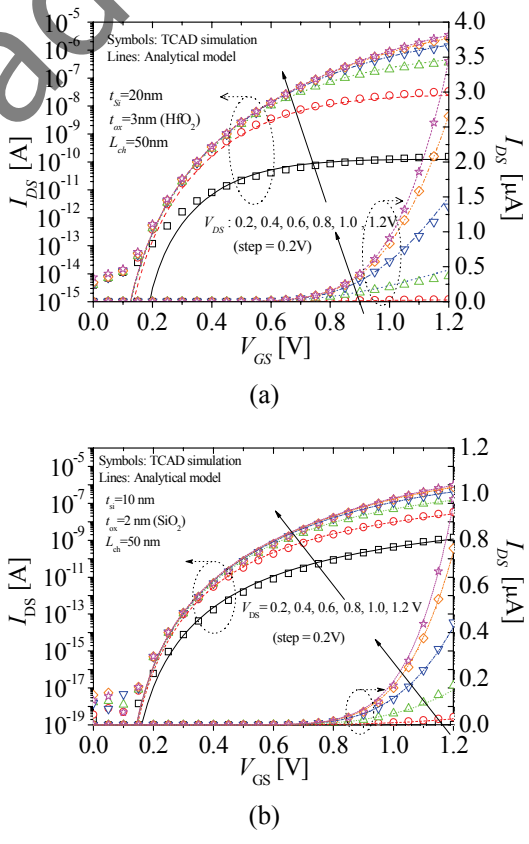

Fig. 3. I_{DS}–V_{GS} characteristics of an (a) n-type SG-TFET and (b) n-type DG-TFET as a function of V_{DS}. Squares (and solid lines), circles (and dot lines), up-triangles (and dash lines), down-triangles (and dash-dot lines), diamond (and dash-dot-dot lines), and stars (and short-dash lines) denote V_{DS} = 0.2, 0.4, 0.6, 0.8, 1.0, and 1.2 V, respectively

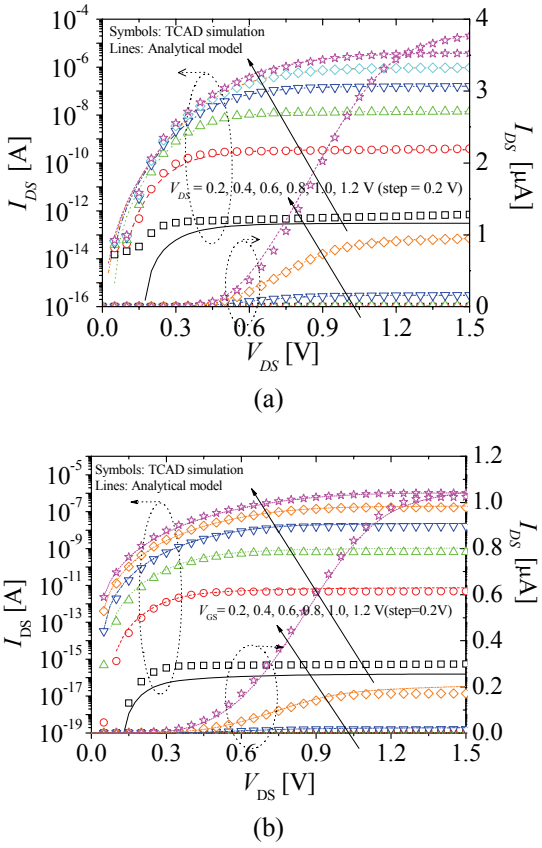

Fig. 4. I_{DS}–V_{DS} characteristics of an (a) n-type SG-TFET and (b) n-type DG-TFET as a function of V_{GS}. Squares (and solid lines), circles (and dot lines), up-triangles (and dash lines), down-triangles (and dash-dot lines), diamond (and dash-dot-dot lines), and stars (and short-dash lines) denote V_{GS} = 0.2, 0.4, 0.6, 0.8, 1.0, and 1.2 V, respectively

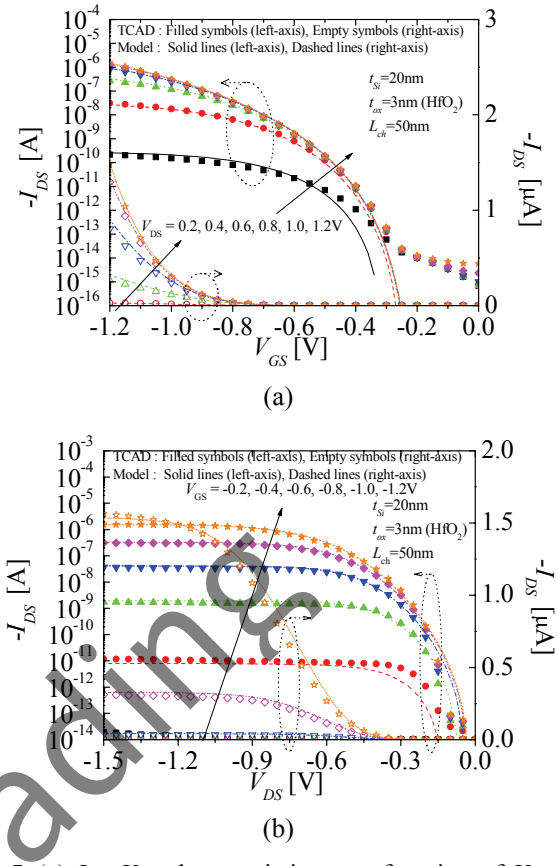

Fig. 5. (a) I_{DS}–V_{GS} characteristics as a function of V_{DS} and (b) I_{DS}–V_{DS} characteristics as a function of V_{GS} of a p-type SG-TFET. Filled symbols and solid lines denote the log plots (left axes), and empty symbols and dashed lines denote the linear plots (right axes). Squares (and solid lines), circles (and dot lines), up-triangles (and dash lines), down-triangles (and dash-dot lines), diamond (and dash-dot-dot lines), and stars (and short-dash lines) denote V_{DS} (V_{GS} in Fig. 5 (b)) = 0.2, 0.4, 0.6, 0.8, 1.0, and 1.2 V, respectively

In order to show the validity of the proposed SG/DG-TFET models in terms of circuit simulation and design, the models were developed with the Verilog-A model in SmartSpice. Using the developed Verilog-A SG/DG-TFET model, a SG-TFET inverter was simulated, consisting of p-type and n-type SG-TFETs in series as shown in the inset in Fig. 6; this is the basic cell of digital integrated circuits. Fig. 6 shows the simulated voltage transfer characteristics (VTC) of the SG-TFET inverter using the developed Verilog-A SG/DG-TFET model in SmartSpice. The figure shows typical inverter characteristics and the effectiveness of the developed Verilog-A model.

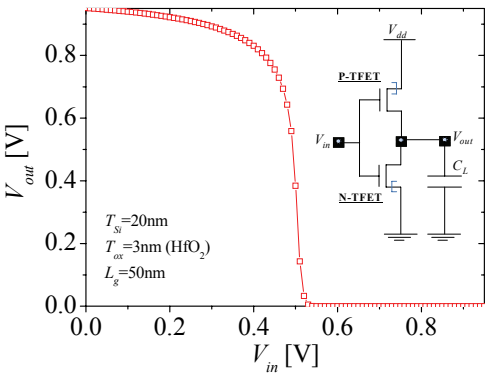

Fig. 6. Verilog-A simulations of VTCs on an SG-TFET inverter as shown in the inset

4. Conclusion

In this study, an analytical expression was derived for the drain–source current of both SG and DG-TFETs on the basis of Kane's BTBT model. The generation rate was integrated over one tunneling direction for the tunneling current, and then the new tunneling current expression was derived using relations including the derivatives of local electric field and potential with respect to the tunneling

direction. In order to compensate for superlinear onset and saturation current with drain voltages, the correction factor with three fitting parameters is used. Three types of TFETs were investigated with simulations of TCAD and the proposed model in order to show that the proposed model is valid for TFETs of different types (n and p), silicon body thicknesses, gate oxide thicknesses, and gate oxide materials. We have shown that the proposed model predicts device characteristics accurately in comparison with TCAD simulation for a large operational range. Compared with the previously developed compact TFET model [19], the proposed model has constant A_k and B_k, which is physics-based [14]. An SG-TFET inverter was simulated with the developed Verilog-A SG/DG-TFET model in the circuit simulator, and the simulation results show typical inverter characteristics.

Acknowledgements

This research was supported by the Ministry of Trade, Industry & Energy (MOTI) (Project No. 10054888) and the Korea Semiconductor Research Consortium(KSRC) support program for the development of future semiconductor devices. This work was supported by IDEC (EDA Tool).

References

[1] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc*., vol. 2, no. 4, pp.44-49, Apr. 2014.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329-337, Nov. 2011.

[3] Q. Huang, R. Jia, C. Chen, H. Zhu, L. Guo, J. Wang, J. Wang, C. Wu, R. Wang, W. Bu, J. Kang, W. Wang, H. Wu, S.-W. Lee, Y. Wang, and R. Huang, "First foundry platform of complementary tunnel-FETs in CMOS baseline technology for ultralow-power IoT applications: Manufacturability, variability and technology roadmap," in *Proc. IEEE Int. Electron Devices Meeting* (*IEDM*), Washington, DC, USA, Dec. 2015, pp. 22.2.1-22.2.4, doi: 10.1109/IEDM.2015.7409756.

[4] M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, and D. Esseni, "Mixed Tunnel-FET/MOSFET Level Shifters: a new proposal to extend the Tunnel-FET application domain," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 3973-3979, Dec. 2015.

[5] D. H. Morris, U. E. Avci, R. Rios, and I. A. Young, "Design of low voltage tunneling-FET logic circuits considering asymmetric conduction characteristics," *IEEE J. Emerg. Sel. Topics Circuits Syst*., vol. 4, no. 4, pp. 380-388, Dec. 2014.

[6] M. G. Bardon, H. P. Neves, R. Puers, and C. V. Hoof, "Pseudo two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827-834, Apr. 2010.

[7] Y. Hong, Y. Yang, L. Yang, G. Samudra, C. H. Heng, and Y. C. Yeo, "SPICE behavioral model of the tunneling field-effect transistor for circuit simulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 12, pp. 946-950, Dec. 2009.

[8] H. Lu, D. Esseni, and A. Seabaugh, "Universal analytic model for tunnel FET circuit simulation," *Solid-State Electronics*, vol. 108, pp. 110-117, 2015.

[9] L. Zhang and M. Chan, "SPICE modeling of double-gate tunnel-FETs including channel transports," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 300-307, Feb. 2014.

[10] M. Gholizadeh and S. E. Hosseini, "A 2-D analytical model for double gate tunnel FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1494-1500, May 2014.

[11] A. Pan and C. O. Chui, "A quasi-analytical model for double-gate tunneling field-effect transistors," *IEEE Electron Device Lett*., vol. 33, no. 10, pp. 1468-1470, Oct. 2012.

[12] C. Wu, R. Huang, Q. Huang, C. Wang, J. Wang, and Y. Wang, "An analytical surface potential model accounting for the dual-modulation effects in tunnel FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2690-2696, Aug. 2014.

[13] A. Pal and A. K. Dutta, "Analytical Drain Current Modeling of Double-Gate Tunnel Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3213-3221, Aug. 2016.

[14] E. O. Kane, "Zener tunneling in semiconductors," *J. Phys. Chem. Solids*, vol. 12, no. 2, pp. 181-188, Jan. 1960.

[15] A. S. Verhulst, D. Leonelli, R. Rooyackers, and G. Groeseneken, "Drain voltage dependent analytical model of tunnel field-effect transistors," *J. Appl. Phys*., vol. 110, no. 2, pp. 024510-1-024510-10, Jul. 2011.

[16] *SmartSpice Manual Ver. 4.18.16.R*, SILVACO International, Santa Clara, CA, 2015.

[17] *ATLAS Manual Ver. 5.20.2.R*, SILVACO International, Santa Clara, CA, 2015.

[18] H. Xu, Y. Dai, N. Li, and J. Xu, "A 2-D semi-analytical model of double-gate tunnel field-effect transistor," *J. Semicond*., vol. 36, no. 5, pp. 1-7, May 2015.

[19] S. F. Najam, M. L. B. Tan, and Y. S. Yu, "General SPICE Modeling Procedure for Double-Gate Tunnel Field-Effect Transistors," *J. Inf. Commun. Converg. Eng.*, vol. 11, no. 1, pp. 115-121, Mar. 2016, doi:10.6109/jicce.2016.14.2.115.

Yun Seop Yu He received the B.S., M.S., and Ph. D. degrees in electronics engineering from Korea University, Seoul, Korea, in 1995, 1997, and 2001, respectively. He is currently a full Professor with Hankyong National University, Anseong, Korea. His research interests include modeling, simulation, and optimization of next generation devices for high performance and low power applications.

Faraz Najam He received his M.S. and Ph.D. degrees from the Department of Electronics and Computer Science, University of Southampton, UK, and Department of Electrical Engineering, Korea University, Seoul, South Korea in 2007 and 2013, respectively. He is currently a research professor with the Dept. of Electrical, Electronic and Control Engineering, Hankyong National University, South Korea as a research professor. His main research interests are in design, fabrication, modeling, and simulation of various emerging logic devices and materials including TFET, 2D materials, MoS2, and graphene.