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# High Step-up DC-DC Converter by Switched Inductor and Voltage Multiplier Cell for Automotive Applications

**Divya Navamani. J†, Vijayakumar. K*, Jegatheeesan. R* and Lavanya. A***

**Abstract** - This paper elaborates two novel proposed topologies (type-I and type-II) of the high step-up DC-DC converter using switched inductor and voltage multiplier cell. The advantages of these proposed topologies are the less voltage stress on semiconductor devices, low device count, high power conversion efficiency, high switch utilization factor and high diode utilization factor. We analyze the Type-I and Type-II topologies operating principle and mathematical analysis in detail in continuous conduction mode. High-intensity discharge lamp for the automotive application can use the derived topologies. The proposed converters give better performance when compared to the existing types. Also, it is found that the proposed type-II converter has relatively higher voltage gain compared to the type-I converter. A 40 W, 12 V input voltage and 72 V output voltage has developed for the type-II converter and the performances are validated.

**Keywords**: High step-up, Switched inductor, Voltage multiplier, Steady state analysis, CCM, DCM, Voltage stress

## 1. Introduction

Various power conditioning circuits use high gain DC-DC converters. Fig. 1 shows the applications of the high gain DC-DC converter. The three broad categories are green energy systems, automotive applications, and electronic equipment. Usage in an automotive application is for boosting the battery voltage (9-12 V) to 100 V required for 35 W High-Intensity Discharge (HID) headlamps [1-2]. The ideal converter topology for this application should meet the following requirements: 1) High efficiency 2) Low input current ripple 3) Lesser number of power semiconductor switches. Conventional boost converter operates with extreme duty ratio to obtain high gain which leads to implications such as current colossal ripples, increased conduction losses, induces severe diode reverse recovery problem, electromagnetic interference problem and increased rating of all components.

The primary research of non-isolated DC-DC converter in the works of literature includes voltage lift techniques, voltage multiplier, coupled inductor and switched inductor/ switched capacitor. F. L. Luo widely used voltage lift technique to achieve high voltage conversion ratio in [3, 4]. Switches incorporated in voltage lift based converters suffer from voltage stress. Isolated converters, such as forward, flyback, half-bridge, full-bridge, and push-pull types can be used to convert a low input voltage into a higher output voltage by adjusting the Transformers' turns ratio. However, the converter active switches suffer from very high voltage stress and high power dissipation due to the leakage inductance of the transformer [5].

Transformerless voltage multipliers widely use Diode-capacitor multipliers. Two-phase interleaved boost converter with voltage multiplier in [6], n stages of diode-capacitor-inductor (D-C-L) unit in [7], combining voltage lift, voltage multiplier, clamp mode and coupled inductor stages in [8], switched capacitor combined with a classical boost converter in [9], connecting n stages of diode-capacitor-inductor (D-C-L) units on the input side and m number of units of voltage multiplier cells in [10], multistage switched-capacitor-voltage-multiplier/divider in [11], interleaved soft switched converter with voltage multiplier in [12], combining coupled inductor and a voltage multiplier module in [13] are used to achieve high gain in the converter. The main disadvantage of combining coupled inductor and a voltage multiplier module is that the duty cycle of each switch shall be not less than 50% under the interleaved control with 180° phase shift. D-C-L unit can be used to achieve high conversion ratio, but the resulting total device number is high. The ESR of the capacitor and parasitic resistance of the inductor affect the efficiency of the converter with voltage lift, voltage multiplier, clamp mode and coupled inductor stages.

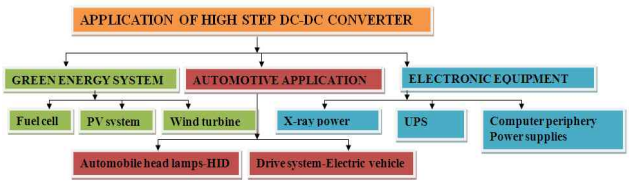


**Fig. 1**. Application of high step up converter

† Corresponding Author: Dept. of Electrical and Electronic Engineering, SRM University, India. (divyateddy1@gmail.com)
* Dept. of Electrical and Electronic Engineering, SRM University, India. (kvijay_srm@rediffmail.com, {jegatheesan. r, lavanya. a}@ ktr. srmuniv. ac. in)
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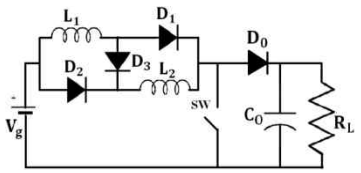
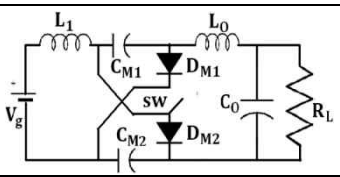
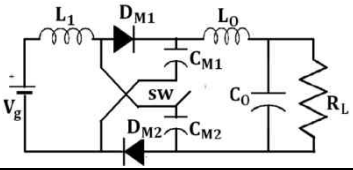
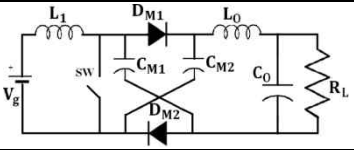
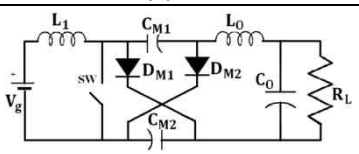
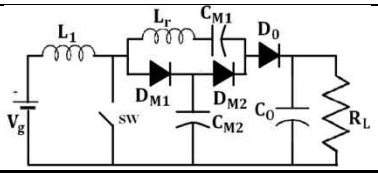
Switched capacitor combined with a classical boost converter and with many numbers of capacitor and diodes achieve high conversion ratio. The drawback of combining n stages of diode-capacitor-inductor (D-C-L) units on the input side and m units of voltage multiplier cells results in high input current ripple. Multistage switched-capacitor-voltage-multiplier/divider needs a complicated control circuit for multiphase operation. Many works on soft switching of DC-DC converter using voltage multiplier cells are carried out in [12, 13]. A family of dc-dc converters based on the three-state switching cell and voltage multiplier cells are proposed in [14]. The Voltage multiplier is integrated multiphase converters are proposed in [15]. Interleaved Dual coupled inductor with voltage multiplier is designed in [16, 17]. Switched Inductor based Active Network Converter (SL-ANC) is used to derive Coupled inductor based Active Network Converter (CL-ANC) and its performance is studied in [18]. However, the static gain of the converter is not much high compared to the other converters.

DC-DC converter with switched capacitor and inductor cell was proposed for step down and step up converter respectively in [19]. However, the voltage stress across the switch is equal to the output voltage which is similar to the quadratic boost converter. A modified form of the converter in [19] is proposed in [20]. Even though the voltage gain is improved; the voltage stress across the switch is still high. The voltage gain of the switched capacitor converter is high, but the output voltage is not regulated. The switched-capacitor converters, proposed in [21] can provide any high conversion ratio. However, they operate with a relatively small efficiency as discussed in [22, 23]. Theoretical performance of switched-capacitor Quadratic converter in [24] provides large voltage conversion ratio, but the voltage and current stress on the power switches are quite high. DC-DC voltage multiplier circuit studied by Fibonacci weighed graph approach is discussed in [25]. Its output voltage is also not regulated.

A study is performed on series of Voltage-Lift (VL) split-inductor-type boost converters in [26, 27]. This transformerless high step-up DC-DC converter requires a significant number of the component count to obtain high

**Table 1**: Boost converters topologies with SL/VM cell

| Topology | Boost converter with single SL/VM cell | Voltage Gain ($G_V$) | Voltage stress across the active switch |
|---|---|---|---|
| TP1 |  | $\frac{1+D}{1-D}$ | $V_0$ |
| TP2 |  | $-\frac{1+D}{1-D}$ | $V_0$ |
| TP3 |  | $-\frac{1+D}{1-D}$ | $V_0$ |
| TP4 |  | $\frac{1+D}{1-D}$ | $\frac{V_0}{1+D}$ |
| TP5 |  | $-\frac{1+D}{1-D}$ | $\frac{V_0}{1+D}$ |
| TP6 |  | $\frac{M+1}{1-D}$ | $\frac{V_0}{M+1}$ |

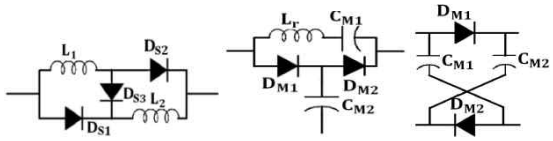
voltage gain. Self-lift and double self-lift Positive Output Elementary Luo (POEL) converters are proposed in [28] by combining voltage lift technique and switched inductor cell for enhancing DC-DC boost the ability of the traditional converters. Super lift boost converter proposed in [29]. However, the voltage conversion ratio is not high enough. Passive and active switched inductor cell is proposed in [30] with equal and unequal inductance in SL cell shows reduced voltage stress, whereas the voltage gain is not too high. From the literature survey, it is concluded that it is necessary to design a converter with all the advantages as mentioned above. The aim of this study is to design a high gain dc-dc converter with low voltage stress across semiconductor devices to provide a constant voltage for steady state operation of HID lamps. To achieve this objective, the high step-up DC-DC converter is designed by combining switched inductor cell and voltage multiplier cell and the performance is analyzed. Two topologies Type-I and Type-II are derived by varying the structure of the voltage multiplier cell. The proposed converters have high voltage gain, less voltage stress with lesser device count.

The paper is organized as follows: The proposed Type-I and Type-II converters are given in section 2. Operating principle and steady state analysis of type- I and type-II topology are described in Article 3 and 4 respectively. Advantages of the proposed converters are furnished in section 5. The simulation and experimental results are presented in section 6. Finally, conclusions are given in section 7. The following assumptions are made for steady state analysis of proposed converters: 1) Components in the converters are ideal, i. e., the ON-state resistances of the active switches, 2) The forward voltage drop of the diodes are ignored and 3) The ESRs of the inductors and capacitors are ignored.

The different topologies of the boost converter with single SL/VM cell and their corresponding voltage gain and voltage stress across the active switch are given in Table 1. The voltage gain of the TP1-TP5 is similar and less compared to TP6. The voltage stress across the active switch of TP1-TP3 is equal to the output voltage which is similar to the conventional boost converter. About voltage gain and switch stress TP6 is best compared to other topologies. TP2, TP3, and TP4 gives negative output voltage.

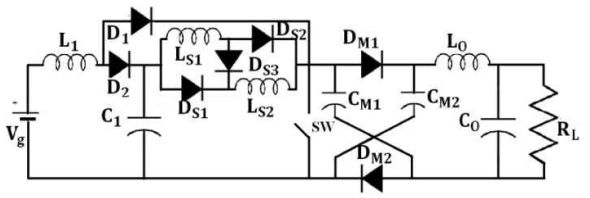
## 2. Proposed Type-I and Type-II Topologies

The switched-inductor cell consists of two inductors ($L_{S1}$,$L_{S2}$), three diodes ($D_{S1}, D_{S2}, D_{S3}$) as shown in Fig. 2(a). The voltage gain can be increased by the transition from parallel to the series connection of inductors in switched inductor cell (SL) during on and off the active switch of the converter respectively. During the on period of the active switch, the inductors in the SL cell are charged in parallel. During the off period of the active switch, the inductors

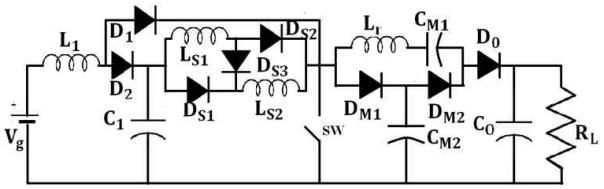



(a) (b) (c)

**Fig. 2.** (a) SL-Switched-inductor cell: (b) $VM_1$; (c) $VM_2$-Voltage multiplier cell




(a)




(b)

**Fig. 3**. Proposed Topologies: (a) Type-I; (b) Type-II

in the SL cell are discharged in series to the load. The step up SL cell can be combined with the boost converters, to get a step-up function [19, 24]. Fig. 2(b) and(c) shows the Voltage multiplier cell consist of two capacitance ($C_{M1}$,$C_{M2}$) and two diode ($D_{M1}$,$D_{M2}$). Voltage gain of any primary converter can be increased by adding VM cell. The voltage conversion ratio is directly proportional to the number of multiplier cell (M), and the voltage stress is inversely proportional to M.

A high voltage gain can be achieved by combining SL and VM cell. Fig. 3(a) shows the circuit configuration of the proposed Type-I converter, which consists of an active switch (SW), inductor $L_1$, switched inductor cell which consists of two inductor ($L_{S1}$, $L_{S2}$), three diodes ($D_{S1}, D_{S2}, D_{S3}$), Voltage multiplier cell consist of two capacitance ($C_{M1}$, $C_{M2}$) and two diodes ($D_{M1}$, $D_{M2}$) and output filter inductor $L_O$. Fig. 3(b) shows the topology of the proposed Type-II converter, which consists of main switch SW, an input inductor $L_1$, Diode ($D_1, D_2$) and a switched inductor cell which consists of two inductor ($L_{S1}$,$L_{S2}$), three diodes ($D_{S1}, D_{S2}, D_{S3}$), Voltage multiplier cell consist of two capacitance ($C_{M1}$, $C_{M2}$), two diode ($D_{M1}$,$D_{M2}$) and resonance inductor $L_r$, output diode $D_O$ and output capacitor $C_O$.

## 3. Operating Principle and Steady Analysis of Type-II topology

The proposed type-I converter can be operated in CCM

and DCM modes.

### 3.1 Operating modes of type-I converter in CCM mode:

The operating modes in CCM can be divided into two modes during one switching cycle.

**Mode 1**[$t_0$,$t_1$]: From time $t_0$ to $t_1$, switchSW is turned on. Diodes $D_1$,$D_{S1}$ and $D_{S2}$ are turned on while diodes $D_2$,$D_{S3}$,$D_{M1}$ and $D_{M2}$ are turned off. The operation of the converter in this mode is shown in Fig. 4(a). The energy of the dc source $V_g$ is transferred to the inductor $L_1$ through the diode $D_1$ and the voltage across the input inductor $L_1$ is $V_g$. The input current $i_g$ is equal to $i_{D1}$ and it increases. The inductors in the switched inductor cell ($L_{s1}$ and $L_{s2}$) are in parallel, and they are charged from capacitor $C_1$. Inductor $L_O$ is charged through SW from the voltage multiplier capacitor $C_{M1}$and $C_{M2}$. For atime $t_0$ to $t_1$, the switch *S*W is turned on, and the following equations can be written from Fig. 4(a)

Voltage across input inductor $L_1$, $V_{L1} = V_g$ (1)

Voltage across switched inductor $L_{S1}$ and $L_{S2}$,

$$V_{LS1} = V_{LS2} = V_{C1} \quad (2)$$

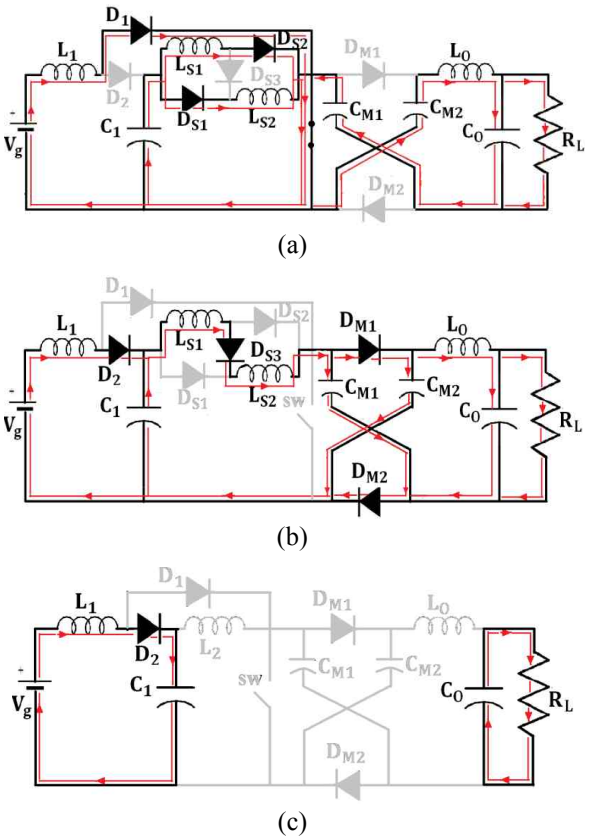



**Fig. 4**. Equivalent circuit of proposed Type-I converter: (a) Mode-I in CCM; (b) Mode-II in CCM; (c) DCM

Voltage across output inductor $L_O$,

$$V_{LO} = 2V_{CM1} - V_O \quad (3)$$

**Mode 2** [$t_1$,$t_2$]: During this time interval, switch SW is turned off. Diodes $D_2$,$D_{S3}$,$D_{M1}$ and $D_{M2}$ are turned on while diodes $D_1$, $D_{S1}$ and $D_{S2}$ are turned off. The operation of the converter in this mode is shown in Fig. 4(b). Inductor $L_1$ delivers the stored energy to capacitor $C_1$, while the inductors in the switched inductor cell ($L_{s1}$ and $L_{s2}$) are in series and their energy is delivered to the capacitor $C_{M1}$. Therefore, the switch voltage is equal to the $C_{M1}$, capacitor voltage. Inductor $L_O$ delivers the stored energy to output. During Mode II, the following equations can be written as

Voltage across input inductor $L_1$, $V_{L1} = V_g - V_{C1}$ (4)

Voltage across switched inductors $L_{S1}$and $L_{S2}$,

$$V_{LS1} = V_{LS2} = \frac{V_{C1} - V_{CM1}}{2} \quad (5)$$

Voltage across output inductor $L_O$, $V_{LO} = V_{CM1} - V_O$ (6)

### 3.2 Steady state analysis of type-I converter in CCM mode:

The voltage and current waveforms of the proposed type-I topology in CCM mode are shown in Fig. 5. Voltage gain of the converter is obtained by applying a volt-second balance on the inductor $L_1$, $L_{S1}$, $L_{S2}$ and $L_O$

$$\int_0^{DT_s} V_g dt + \int_{DT_s}^{T_s} (V_g - V_{C1}) dt \quad (7)$$

$$\int_0^{DT_s} V_{C1} dt + \int_{DT_s}^{T_s} \left(\frac{V_{C1} - V_{CM1}}{2}\right) dt \quad (8)$$

$$\int_0^{DT_s} (2V_{CM1} - V_O) dt + \int_{DT_s}^{T_s} (V_{CM1} - V_O) dt \quad (9)$$

By simplifying (7), (8) and (9) we can derive the voltage conversion ratio as

$$G_{V-CCM} = \frac{V_O}{V_g} = \left[\frac{1+D}{1-D}\right]^2 \quad (10)$$

The generalized voltage transfer gain for even and odd number of voltage multiplier cell is

$$G_{V(M=2,4,6....)} = \frac{[(M+1) - D][1+D]}{[1-D]^2} \quad (11)$$

$$G_{V(M=1,3,5....)} = \frac{[M+D][1+D]}{[1-D]^2} \quad (12)$$

Where M is the number of multiplier cell.

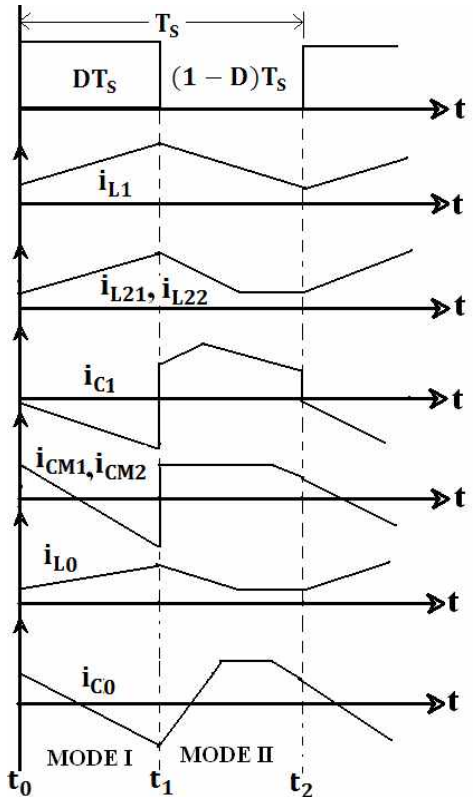



**Fig. 5** Current and voltage waveforms of the proposed Type-I converter

Inductor current equation is obtained by using the ampere-second principle on capacitors $C_1, C_{M1}, C_{M2}$

$$\int_0^{DT_s} -2i_{L21}\,dt + \int_{DT_s}^{T_s} (i_{L1} - i_{LS1})dt \tag{13}$$

$$\int_0^{DT_s} -i_{LO}\,dt + \int_{DT_s}^{T_s} \left(\frac{i_{LS1} - i_{LO}}{2}\right) dt \tag{14}$$

Combining (13) and (14) we can derive the following inductor current equations

$$i_{L1} = \frac{V_O}{R_O}\left[\frac{1+D}{1-D}\right]^2 \tag{15}$$

$$i_{LS1} = i_{LS2} = \frac{V_O}{R_O}\left[\frac{1+D}{1-D}\right] \tag{16}$$

### 3.3 Operating modes and Steady state analysis of type-I converter in DCM mode:

The current through the diode $D_{S3}$ reduces to zero during the off period, and the circuit operates in DCM mode. Current through the inductors $L_{S1}$ and $L_{S2}$ is equal to $i_{DS3}$. There are three modes of operation. During the first mode, the voltage across inductors $L_1$, $L_{S1}$, $L_{S2}$ and $L_O$ are similar to those in mode I of CCM operation. In the second mode, the voltage across inductors $L_1$, $L_{S1}$, $L_{S2}$ and $L_O$ are similar to those in mode II of CCM operation. The current $i_{LS1}$ and $i_{DS3}$ reduces to zero before the end of mode II. The equivalent circuit of this mode is shown Fig. 4(c) wherein output capacitor supplies the load.

The variation ratio of inductor current,

$$i_{LS1} = \frac{\Delta i_{LS1}/2}{I_{LS1}} = \frac{R_L D[1-D]^2}{2L_{S1}f_s[1+D]^3} \tag{17}$$

During switching off period the variation of $i_{DS3}$ is equal to $\Delta i_{LS1}$. The variation ratio of the current $i_{DS3}$ is one when the circuit works in the boundary state. Equating (17) to one.

$$\frac{D[1-D]^2}{2[1+D]^3}\frac{R_L}{L_{S1}f_S} = 1 \tag{18}$$

Simplifying (18) the boundary condition between CCM and DCM is

$$G_{Bou} = \frac{DR_L}{2[1+D]L_{S1}f_S} \tag{19}$$

When the voltage gain is greater than $G_{Bou}$ the circuit operates in DCM mode. In this case, current through the diode $D_{S3}$ reduces to zero at $t_2 = [D + (1-D)k]T$, where k is the current filling factor given by

$$k = \frac{2[1+D]^3 L_{S1}f_S}{D[1-D]^2 R_L} \tag{20}$$

In the DCM, by applying the volt-second balance principle

$$\int_0^{DT_s} V_g dt + \int_{DT_s}^{(1-D)kT_s} (V_g - V_{C1})dt \tag{21}$$

$$\int_0^{DT_s} V_{C1} dt + \int_{DT_s}^{(1-D)kT_s} \left(\frac{V_{C1} - V_{CM1}}{2}\right) dt \tag{22}$$

$$\int_0^{DT_s} (2V_{CM1} - V_O)dt + \int_{DT_s}^{(1-D)kT_s} (V_{CM1} - V_O)dt \tag{23}$$

Combining the Eqs. (21), (22) 1nd (23), we can get

$$\frac{V_O}{V_g} = \left[1 + \frac{2D}{[1-D]k}\right]^2 \tag{24}$$

Substituting (20) into (24) yields, the voltage transfer gain in the DCM mode as

$$G_{V-DCM} = \left[1 + \frac{D^2[1-D]R_L}{[1+D]^3 L_{S1}f_S}\right]^2 \tag{25}$$

## 4. Operating Principle and Steady State Analysis of Type-II Topology

### 4.1 Operating modes of Type-II converter in CCM mode

The operating modes can be divided into seven modes during one switching cycle. The equivalent circuit in CCM operation is shown in Fig. 6(a)-(e).

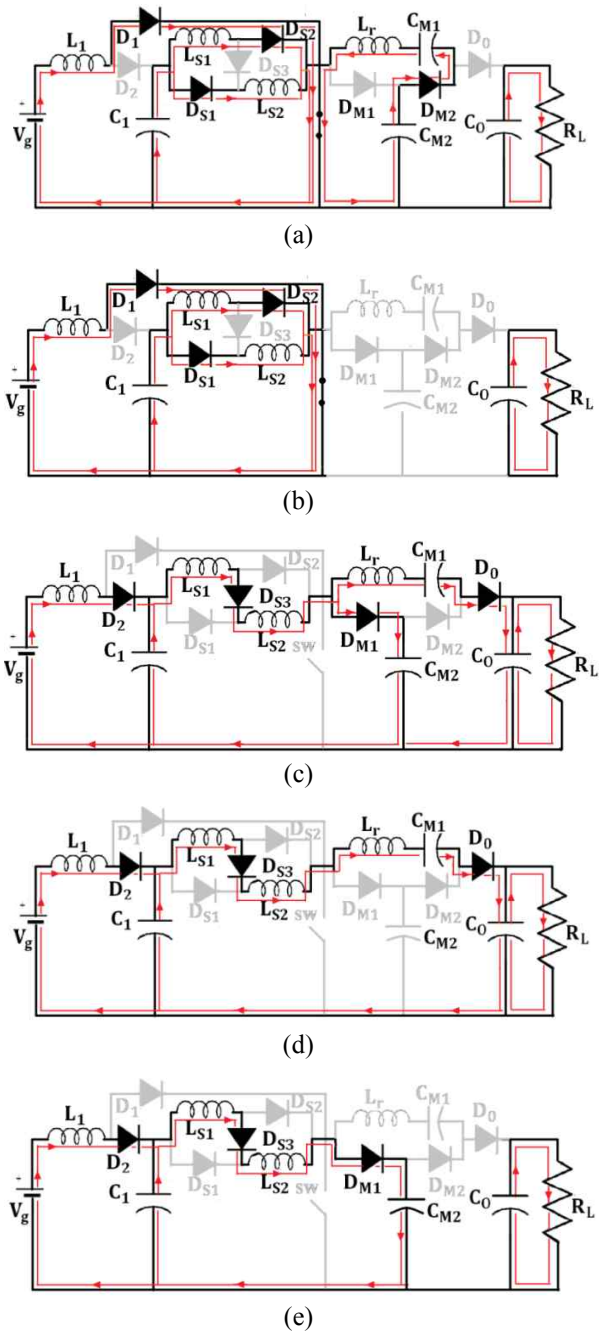



**Fig. 6**. Equivalent circuit of proposed Type-II converter: (a), -(e) CCM- (a) Mode-I; (b) Mode-II; (c) Mode-III,VI,VII; (d) Mode-IV; (e) Mode-V

**Mode I** $[0,t_0]$: The switch SW is conducting at this mode. The current flow path is shown in Fig. 6(a). The input inductor $L_1$ is charged by the input DC voltage source $V_g$ and the inductors in the SL cell are charged in parallel by the capacitor $C_1$. The capacitors $C_{M1}$ and $C_{M2}$ are charged to the output voltage of the quadratic boost converter with switched inductor cell $(V_g[1+D]/[1-D]^2$ through the diode $D_{M2}$. The average voltages of $C_{M1}$ and $C_{M2}$ are equal.

**Mode II** $[t_0,t_1]$: During this mode the switch SW is on state. At this instant $(t_0)$ diode $D_{M2}$ turns off. The current flow path is shown in Fig. 6(b). The input inductor $L_1$ is charged by the input DC voltage source $V_g$ and the inductors in the SL cell are charged in parallel by the capacitor$C_1$. It is similar to Quadratic boost converter in conducting state. The inductors $L_1$, $L_{S1}$, $L_{S2}$ stores energy until the switch SW turns off at the instant $(t_1)$.

**Mode III, V, VII** $[t_1,t_2]$: At this instant $(t_1)$, switch SW turns off, Diodes $D_2, D_{M1}$ and $D_O$ turn on and the energy stored in the inductors $L_1$, $L_{S1}$, and $L_{S2}$ are transferred to the output capacitor $C_O$ through the diode $D_O$. The energy is also transferred to the capacitor $C_{M2}$ through the diode $D_{M1}$ and to the capacitor $C_1$ through the diode $D_2$. The modes 5 and 7 are just similar to mode III. The current flow path is shown in Fig. 6(c).

**Mode IV** $[t_2,t_3]$: During this mode the switch SW is in off state. At this instant $(t_2)$ diode $D_{M1}$ turns off. The current flow path is shown in Fig. 6(d). The energy stored in the inductors $L_1$, $L_{S1}$, and $L_{S2}$ is transferred to the output capacitor$C_O$ through the diode$D_O$. At the end of this mode $(t_3)$ diode $D_{M1}$ turns on again and enters into the mode similar mode 3.

**Mode V** $[t_4,t_5]$: At this instant $(t_4)$ diode $D_O$ turns off. The current flow path is shown in Fig. 6(e). The energy stored in the inductors $L_1$, $L_{S1}$, and $L_{S2}$ is transferred to the output capacitor $C_{M2}$ through the diode $D_{M1}$. At the end of this mode $(t_5)$ diode $D_O$ turns on again and enters in to the mode similar to mode 3. Fig. 7 shows some typical waveforms obtained during continuous conduction mode (CCM)

### 4.2 Steady state analysis of Type-II converter in CCM mode

To simplify the analysis only stages 1 and 3 are considered for CCM operation because the time durations of modes 4 and 6 are short. Modes 3, 5 and 7 are similar. At mode 1, the main switch SW is turned ON, the inductor $L_1$is charged by the input DCvoltage source $V_g$, and the inductors in the switched inductor cells are charged by the voltage across $C_1$.

The following equations are obtained from Fig. 6(a)

$$V_{L1} = V_g \tag{26}$$

$$V_{LS1} = V_{LS2} = V_{C1} \tag{27}$$

During mode 3, the main switch SWis in the OFF state, the inductor $L_1$ and switched inductor cell's inductors $L_{S1,}$ and $L_{S2}$ are discharged, respectively. The voltages across the inductors $L_1$ and $L_{S1,}L_{S2}$ are

$$V_{L1} = V_g - V_{C1} \quad (28)$$

$$V_{LS1} = V_{LS2} = \frac{V_{C1}-V_{CM1}}{2} \quad (29)$$

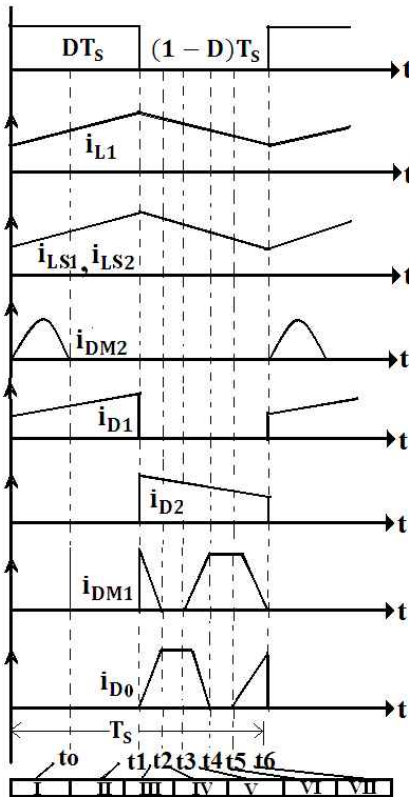



**Fig. 7** Current and voltage waveforms of the proposed Type-II converter

During the mode 1 capacitor $C_{M2}$ is charged with the output voltage of quadratic boost converter with voltage multiplier cell. After mode 4, the output voltage is equal to two times of capacitor voltage $C_{M2}$ for one multiplier cell [M=1]. Thus

$$V_O = 2V_{CM2} \quad (30)$$

Applying a volt-second balance on the inductors $L_1$, $L_{S1}$, $L_{S2}$ yields

$$\int_0^{DT_s} V_g dt + \int_{DT_s}^{T_s} (V_g - V_{C1}) dt \quad (31)$$

$$\int_0^{DT_s} V_{C1} dt + \int_{DT_s}^{T_s} \left(\frac{V_{C1}-V_{CM1}}{2}\right) dt \quad (32)$$

$$\int_0^{DT_s} (2V_{CM1} - V_O) dt + \int_{DT_s}^{T_s} (V_{CM1} - V_O) dt \quad (33)$$

By simplifying (31),(32) and (33), voltage gain in CCM is obtained as

$$G_{V-CCM} = \frac{V_O}{V_g} = \frac{[M+1][1+D]}{[1-D]^2} \quad (34)$$

## 5. Advantages of the Proposed Converters

The proposed converter is compared to some of the recently introduced high step-up converter in the literature [7, 29, 30]. The following parameters are compared: voltage gain, voltage stress across switches and diodes, switch and diode utilization factor, and total device count. The results are tabulated in Tables 2 and 3.

### 5.1 Voltage gain

The voltage gains of the proposed converter type-I and

**Table 2**. Comparison of proposed and other high gain converters in literature

| Sno | | Super – lift boost converter[29] | | | SH-SLC[30] | | | Converter with D-C-L Unit[7] | | | Proposed converter | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | Type-I | | | Type-II | | |
| 1 | no of switches | 1 | | | 2 | | | 1 | | | 1 | | | 1 | | |
| 2 | no of inductor | 4 | | | 4 | | | 3 | | | 4 | | | 3 | | |
| 3 | no of diode | 10 | | | 7 | | | 7 | | | 7 | | | 8 | | |
| 4 | no of capacitor | 1 | | | 1 | | | 5 | | | 4 | | | 4 | | |
| 5 | Total components | **16** | | | **14** | | | **16** | | | **16** | | | **16** | | |
| 6 | Voltage gain($G_V$) | $\frac{1+3D}{1-D}$ (q = 3) | | | $\frac{1+3D}{1-D}$ | | | $\frac{5+D}{1-D}$ (n = 2) | | | $\left[\frac{1+D}{1-D}\right]^2$ | | | $\frac{[1+D][M+1]}{[1-D]^2}$ | | |
| 7 | Duty cycle | 0.3 | 0.5 | 0.7 | 0.3 | 0.5 | 0.7 | 0.3 | 0.5 | 0.7 | 0.3 | 0.5 | 0.7 | 0.3 | 0.5 | 0.7 |
| 8 | Gain $\left[\frac{V_O}{V_g}\right]$ | 2.7 | 5 | 10.3 | 2.7 | 5 | 10.3 | 7.5 | 11 | 19 | 3.4 | 9 | 32 | 5.3 | 12 | 37.7 |
| 9 | Voltage stress of switch | $V_O$ | | | $\frac{V_O+V_g}{2}$ | | | $\frac{V_O+V_g}{2}$ | | | $\frac{V_O}{1+D}$ | | | $\frac{V_O}{M+1}$ | | |
| 10 | Voltage stress across diode in SL cell | $\frac{V_O-V_g}{4}$ (q = 3) | | | $\frac{V_O-V_g}{4}$ | | | $\frac{V_O+V_g}{3}$ (n = 2) | | | $\frac{V_O D}{G_V[1-D]^2}$ | | | $\frac{V_O D}{G_V[1-D]^2}$ | | |
| 11 | Voltage stress across output diode | $V_O - V_g$ | | | $V_O - V_g$ | | | $\frac{V_O+V_g}{2}$ | | | Does not exist | | | $\frac{V_O}{M+1}$ | | |
| **$V_g$ = 12 V $V_O$=144 V** | | | | | | | | | | | | | | | | |
| 12 | Duty cycle | 0.73 | | | 0.73 | | | 0.538 | | | 0.55 | | | 0.5 | | |

type-II are compared with the converters in [7, 29, 30]. It is found that voltage gain of the type-I and type-II converters are very high for almost various duty ratio. The voltage gain of type-II is larger when compared to type-I. Fig. 8(a) shows the voltage gain ($G_V$) against the duty ratio of the proposed converter and converters in [7, 29, 30] at CCM

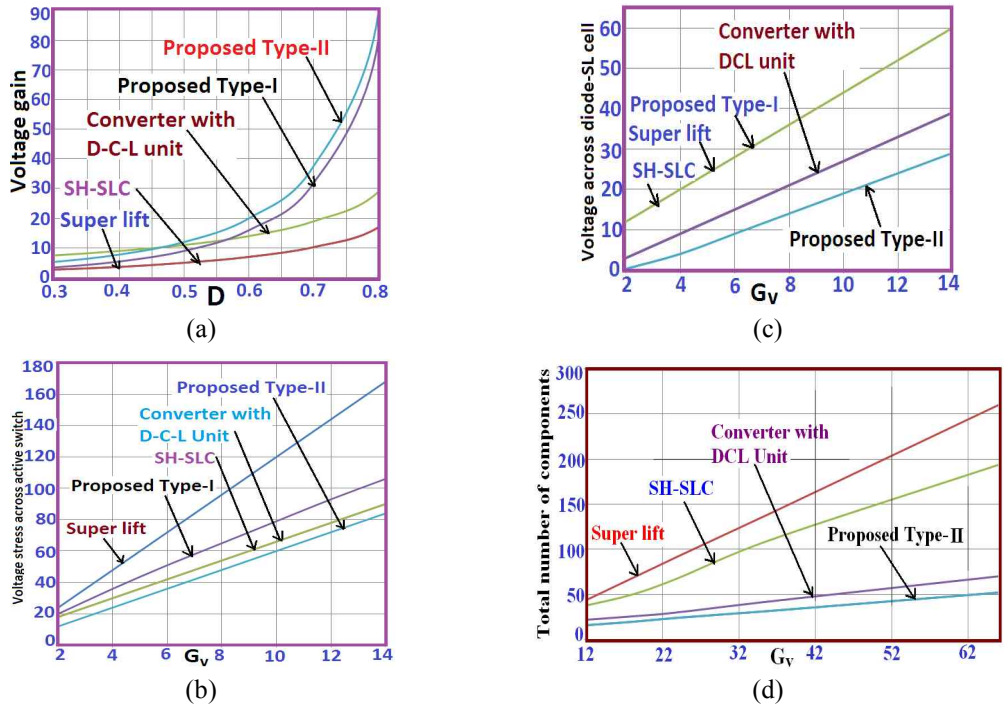



**Fig. 8.** (a) Comparison of voltage gain; (b) Comparison of voltage stress across active switch; (c) Comparison of voltage stress across the diode in SL cell; (d) Comparison of total device count

**Table 3.** Comparison of switch and diode utilization factor

| Sno | | Super - lift boost converter[29] | SH-SLC[30] | Converter with D-C-L Unit[7] | Proposed converter | |
|---|---|---|---|---|---|---|
| | | | | | Type-I | Type-II |
| | **Switch utilization factor( $P_O = 40$ W , $V_g = 12$ V , $V_O$=144 V)** | | | | | |
| 1 | Peak voltage, current | 144V, 2.850A | 78V, 1.422A | 78V, 5.377A | 96V, 3.908A | 72V,3.933A |
| 2 | No of switch | 1 | 2 | 1 | 1 | 1 |
| 3 | SUF | **0.09745** | **0.1803** | **0.0953** | **0.1066** | **0.1412** |
| | **Diode utilization factor- Multiplier cell** | | | | | |
| 4 | Peak voltage, current | (q=3); 1x 33V,1.724A 2x 12V, 2.137A | 2x12V, 1.72A 4x33V,0.712A | (n=2); 2x 52V,1.641A | 2x96V,0.43A | 2x72V,0.393A |
| 6 | No of diode in SL cell | 3 | 6 | 2 | 2 | 2 |
| 7 | DUF | **0.369** | **0.295** | **0.234** | **0.4844** | **0.706** |
| | **Total Diode utilization factor** | | | | | |
| 8 | Peak voltage, current | 3x12V,1.72A 1x132V,1.72A 2x33,0.721A 2x33V,1.42A 2x33V,0.726A | 2x12V,1.72A 1x132V,1.72A 4x33V,0.712A | 4x52V,1.64A 2x78V,0.409A 1x78V,0.378A | 3x24V,0.73A 2x96V,0.43A 1x48V,2.26A 1x24V,2.51A | 3x24V,0.75A 2x72V,0.393A 1x48V,1.67A 1x24V,2.30A 1x72V,0.45A |
| 9 | Total no of diode | 10 | 7 | 7 | 7 | 8 |
| 10 | DUF | **0.0698** | **0.1103** | **0.0920** | **0.1306** | **0.1439** |
| 11 | Generalized Voltage gain | $\frac{1+MD}{1-D}$ | $\frac{1+[4M-1]D}{1-D}$ | $\frac{2M+1+D}{1-D}$ | $G_{V(M=2,4,6\ldots)} = \frac{[(M+1)-D][1+D]}{[1-D]^2}$ $G_{V(M=1,3,5\ldots)} = \frac{[M+D][1+D]}{[1-D]^2}$ | $\frac{[1+D][M+1]}{[1-D]^2}$ |
| 12 | Generalized total device count | 4M+4 | 12M+2 | 4M+10 | 4M+12 | 4M+12 |
| 13 | Components in M cell | 1-inductor 3-diode | 2-switch 4-inductor 6-diode | 1-inductor 2-diode 1-capacitor | 2-diode 2-capacitor | 2-diode 2-capacitor |

operation. The voltage gain of type-II topology is increased by M+1 times of quadratic boost converter, where the M= number of voltage multiplier cell.

### 5.2 Voltage stress across active switch and diodes:

The expression for the average voltage, average current, voltage and current stress on various components of type-I and type-II topologies are shown in Table 4. It is clear from the Fig. 8 (b) the proposed type-II topology has the lowest switch voltage stress compared to the other topologies. Since voltage stress is less compared to other three converters, it allows the use of a low-voltage-rated MOSFET with lower $R_{DS-ON}$ which is beneficial regarding efficiency. Fig. 8(c) shows that the proposed Type-II topology has most moderate voltage stress across the diode in switched inductor cell compared to other converters. This is more advantageous, because it allows the use of fast switching diode for mitigating the reverse recovery problem. It is also found that the current stress of the switch in proposed type-II is less compared to the converter reported in [7]. This is because the main switch in converter [7] is connected in series with the input supply and draws high current for high output power.

### 5.3 Total device count:

The total number components mainly decide the size, weight and cost of the converter in the converter. The comparison between the proposed topology with other converters concerning the number of devices is given in Table 3. To obtain the graphical comparison between the voltage gain and the total device count, the duty cycle is taken as 0.5 for all the converters, where M is the number of multiplier cell. It can be seen from the Fig. 8(d) the proposed converter requires less number of components compared to other converters. It is found that the proposed type-II converter needs lesser total device count to achieve the same voltage conversion ratio as compared to other topologies. Higher power conversion is possible with proposed topology with less device number.

### 5.4 Utilization factor of switching devices:

The comparison has been made in terms of the utilization factor of switching devices for the proposed converter and other switched inductor based converters in Table 3. The switch utilization factor of the proposed type-II converter is the best compared to all other converters except the converter in [30]. Proposed Type-II converter and converter in [30] are the best for diode and switch utilization factor respectively. Diode utilization factor of the multiplier cell is high for proposed Type-II converter. If numbers of cells are increased the diode utilization factor of the proposed converter will be comparatively good compared to other converters. Proposed type-II converter has higher total diode utilization factor as compared to all converters.

### 5.5 Power losses and Efficiency Analysis

Table 4 gives the average and maximum voltage of the semiconductor devices and other components of the proposed Type -II converter.

The average current through the diode can be given by

$$i_{D1avg} = \frac{1}{T}\int_0^{DT} i_{L1}\,dt = i_O\,G_V D \quad (35)$$

$$i_{D2avg} = \frac{1}{T}\int_{DT}^{T} i_{L1}\,dt = i_O\,G_V[1-D] \quad (36)$$

$$i_{Ds1avg} = i_{Ds2avg} = \frac{1}{T}\int_0^{DT} i_{Ls1}\,dt = \frac{i_O[M+1]D}{[1-D]} \quad (37)$$

$$i_{Ds3avg} = \frac{1}{T}\int_{DT}^{T} i_{Ls2}\,dt = i_O[M+1] \quad (38)$$

$$i_{DM1avg} = i_{DM2avg} = i_{DO2avg} = i_O \quad (39)$$

The power loss due to forward voltage drop in diode is given by

$$P_{VF} = V_F[i_{D1avg} + i_{D2avg} + i_{Ds1avg} + i_{Ds2avg} + iDs3avg + iDM1avg + iDM2avg + iD0avg \quad (40)$$

The RMS current through the diode can be given as

$$i_{D1rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{L1}}^2\,dt} = \frac{i_O[1+D][M+1]\sqrt{D}}{[1-D]^2} \quad (41)$$

$$i_{D2rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{Ls1}}^2\,dt} = \frac{i_O[1+D][M+1]\sqrt{1-D}}{[1-D]^2} \quad (42)$$

$$i_{Ds11rms} = i_{Ds11rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{L2}}^2\,dt} = \frac{i_O[M+1]\sqrt{D}}{[1-D]} \quad (43)$$

$$i_{Ds3rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{Ls2}}^2\,dt} = \frac{i_O[M+1]}{\sqrt{1-D}} \quad (44)$$

$$i_{DM1rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{CM2}}^2\,dt} = \frac{i_O\sqrt{1+D}}{\sqrt{1-D}} \quad (45)$$

$$i_{DM2rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{CM2}}^2\,dt} = \frac{2i_O\sqrt{1+D}}{\sqrt{1-D}} \quad (46)$$

$$i_{D0rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{CM1}}^2\,dt} = \frac{i_O\sqrt{1+D}}{\sqrt{1-D}} \quad (47)$$

The power loss in forward resistance $R_F$ of the diode is given as

$$P_{RF} = [{i_{D1rms}}^2 + {i_{D2rms}}^2 + {i_{Ds11rms}}^2 + {i_{Ds2rms}}^2 + iDs3rms2 + iDM1rms2 + iDm2rms2 + iD0rms2RF \quad (48)$$

From Eqn (40), (48) total power loss in diode is obtained

$$P_D = P_{RF} + P_{VF}$$

RMS Current through the switch SW is

**Table 4**: Component voltage and current

| | | Proposed converter | |
|---|---|---|---|
| | | Type-I | Type-II |
| Voltage stress of the diodes in switched inductor cell | $D_{S1}$ | $\frac{V_O D}{G_V[1-D]^2}$ | $\frac{V_O D}{G_V[1-D]^2}$ |
| | $D_{S2}$ | | |
| | $D_{S3}$ | | |
| Voltage stress of the diodes in voltage multiplier cell | $D_{M1}$ | $\frac{V_O}{1+D}$ | $\frac{V_O}{M+1}$ |
| | $D_{M2}$ | | |
| Voltage stress of the diodes in QB | $D_1$ | $\frac{2V_O D}{G_V[1-D]^2}$ | $\frac{2V_O D}{G_V[1-D]^2}$ |
| | $D_2$ | $\frac{V_O}{G_V[1-D]}$ | $\frac{V_O}{G_V[1-D]}$ |
| Voltage stress of the switch | SW | $\frac{V_O}{1+D}$ | $\frac{V_O}{M+1}$ |
| Average voltage of the diodes in switched inductor cell | $D_{S1}$ | $\frac{V_O D}{G_V[1-D]}$ | $\frac{V_O D}{G_V[1-D]}$ |
| | $D_{S2}$ | | |
| | $D_{S3}$ | | |
| Average voltage of the diodes in voltage multiplier cell | $D_{M1}$ | $\frac{V_O D}{1+D}$ | $\frac{V_O D}{M+1}$ |
| | $D_{M2}$ | | $\frac{V_O[1-D]}{M+1}$ |
| Average voltage of the diodes in QB | $D_1$ | $\frac{2V_O D}{G_V[1-D]}$ | $\frac{2V_O D}{G_V[1-D]}$ |
| | $D_2$ | $\frac{V_O D}{G_V[1-D]}$ | $\frac{V_O D}{G_V[1-D]}$ |
| Average current of the diodes in QB | $D_1$ | $G_V I_O D$ | $G_V I_O D$ |
| | $D_2$ | $G_V I_O[1-D]$ | $G_V I_O[1-D]$ |
| Average Inductor current | $L_1$ | $G_V I_O$ | $G_V I_O$ |
| | $L_{S1}=L_{S2}$ | $\sqrt{G_V} I_O$ | $\frac{I_O[M+1]}{[1-D]}$ |
| Average current of the diodes in switched inductor cell | $D_{S1}$ | $\sqrt{G_V} I_O D$ | $\frac{I_O[M+1]D}{[1-D]}$ |
| | $D_{S2}$ | | |
| | $D_{S3}$ | $\sqrt{G_V} I_O[1-D]$ | $I_O[M+1]$ |
| Average current of the diodes in voltage multiplier cell | $D_{M1}$ | $\frac{\sqrt{G_V} I_O[1+D]-I_O[3D-1]}{2}$ | $I_O$ |
| | $D_{M2}$ | | |
| RMS current of the switch | SW | $\sqrt{G_V}[2+\sqrt{G_V}]I_O D$ | $\frac{I_O[M+1][3-D]\sqrt{D}}{[1-D]^2}$ |

$$i_{SW\ rms}=\sqrt{\frac{1}{T}\int_0^{DT}[i_{L1}+2i_{Ls1}]^2\,dt}$$

Hence, ohmic power loss in switch is

$$P_{R(on)}=i_{SW}{}^2 r_{DS}=\frac{i_O[M+1][3-D]\sqrt{D}}{[1-D]^2}r_{DS} \quad (49)$$

Switching loss in the switch is obtained by

$$P_{SW}=\frac{1}{2}f_s C_O R_O P_O \quad (50)$$

From Eqn (49),(50) total losses in a switch is obtained. RMS value of the inductor current can be derived as

$$i_{L1rms}=i_O G_V; i_{Ls1rms}=i_{Ls2rms}=\frac{i_O[M+1]}{[1-D]}; \quad (51)$$

Power loss associated with inductor can be derived using

$$P_L=i_{L1rms}{}^2 r_{L1}+i_{Ls1rms}{}^2 r_{Ls1}+i_{Ls2rms}{}^2 r_{Ls2} \quad (52)$$

Capacitor current RMS values can be given by

$$i_{C1rms}=\frac{2i_O D}{[1-D]^3}; \quad (53)$$

$$i_{CM1rms}=i_{CM2rms}=\frac{2i_O\sqrt{1+D}}{\sqrt{1-D}} \quad (54)$$

$$i_{CO rms}=\frac{i_O\sqrt{D}}{[1-D]} \quad (55)$$

Capacitor power losses can be derived from

$$P_C=i_{C1rms}{}^2 r_{C1}+i_{CM1rms}{}^2 r_{CM1}+i_{CM2rms}{}^2 r_{CM2}+i_{CO rms}{}^2 r_{CO} \quad (56)$$

Total power loss in the converter is

$$P_{LOSS}=P_{R(on)}+P_{SW}+P_D+P_L+P_C \quad (57)$$

The efficiency of the proposed high step up converter is given by

$$\text{Efficiency} = \eta = \frac{P_0}{P_h}\frac{1}{1+(P_{Loss}/P_0)} \quad (58)$$

## 6. Simulated and Experimental verification

The effectiveness of the proposed type-II converter is designed and tested for 12V input voltage, 72V output voltage, 40W to verify the theoretical analysis. The following are the hardware components used for constructing the prototype:

1. MOSFET, STN1NF10
2. Diode $D_1, D_2$ −1N5401, 100V, 3A
3. Multiplier diodes-1N5817-100V, 1A
4. Microcontroller-PIC16F877(PWM controller)

### 6.1 Design of inductor:

The expression for the design of inductor is derived as follows:

During the on period of switch (SW), input current ripple is given as,

$$\Delta i_{L1} = \frac{V_g DT}{L_1} \quad (59)$$

From Eqn (59), value of inductor $L_1$ is obtained by

$$L_1 > \frac{[1-D]^4 DR_{Om\,ax}}{2[M+1]^2[1+D]^2 f_s} \quad (60)$$

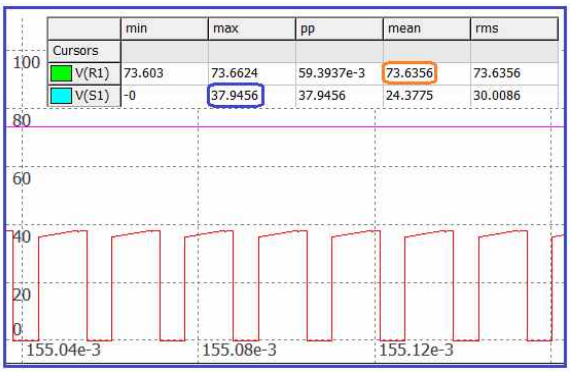
$$\Delta i_{LS1} = \Delta i_{LS2}\frac{V_{C1}DT}{L_{S1}} \quad (61)$$

From eqn (61) value of inductor $L_{s1}$ and $L_{s2}$ is obtained by

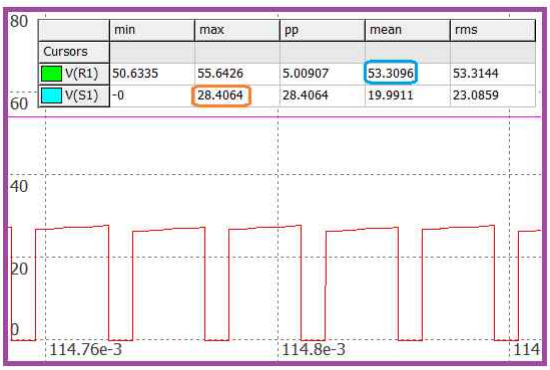
$$L_{s1} = L_{s2} > \frac{[1-D]^2 DR_{Om\,ax}}{2[M+1]^2[1+D]f_s} \quad (62)$$

### 6.2 Design of Capacitor:

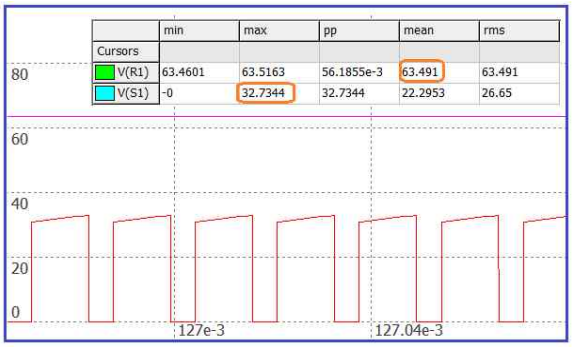
The values of the input and output capacitors depend on the output voltage, load resistance, and the operating frequency.



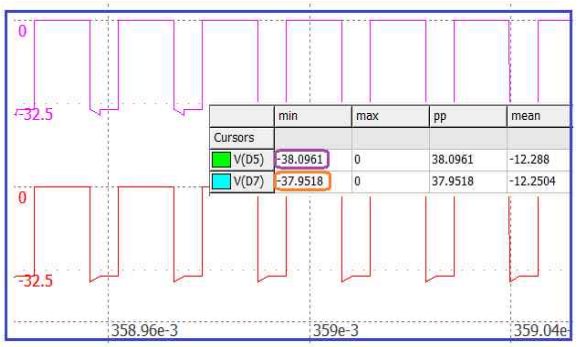

(a)




(c)




(b)




(d)

**Fig. 9** Simulation results (a) Output voltage and switch voltage for D= 0. 34 (b) Output voltage and switch voltage for D= 0. 3 (c) Output voltage and switch voltage for D= 0. 25 (d) Voltage multiplier ($D_{M1}$) and output diode ($D_O$)voltage waveform = $\frac{V_o}{M+1}$ = 37 V for D=0. 34

$$C > \frac{V_O D_{max}}{R_{Lmin} f_s} \quad (63)$$

Satisfying (63) input and output capacitor are selected as 22uF.

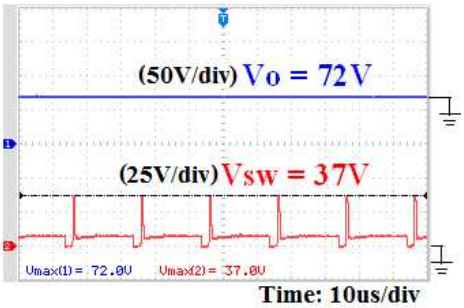
The value of voltage multiplier capacitor depends on maximum power, multiplier capacitor voltage and operating frequency. Thus

$$C_{M1} > \frac{P_{Omax}}{V_{CM1}^2 f_s} \quad (64)$$

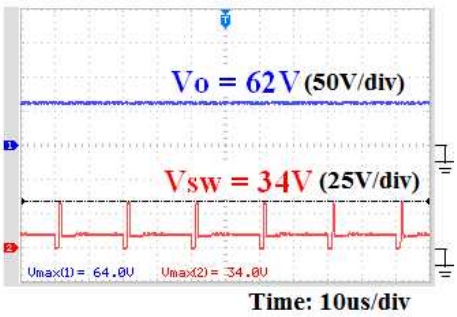
From (64) voltage multiplier capacitor is selected as 0. 5uF.

Simulation is carried in the nl5 simulator. The obtained output voltage, voltage stresses across switches and diodes are shown given in Fig. 9(a)-(d).

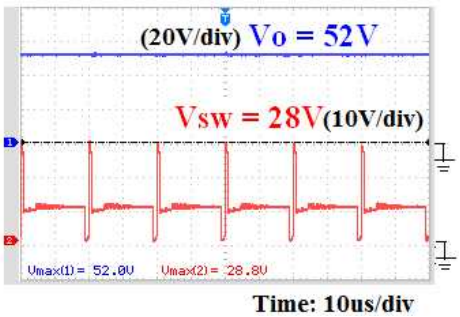
The experimental waveforms with different duty cycle are shown in Fig. 10(a)-(c). Further, Fig. 10(a)-(c) show the output voltage and voltage stress on the switch for different duty cycles. It is proved that the switch stress is equal to $V_o/(M+1)$. It means that the voltage stress across the switch is low, i. e., half of the output voltage with M=1, when the switch is turned off. From the Fig. 10(d), it is proved that the maximum voltage across multiplier diode is also half of the output voltage. The Photograph of the constructed proposed -type-II topology is shown in Fig. 10(e). Table 6 gives the comparison of the efficiency of proposed type-II converter with other high step-up converters taken for comparison. The maximum measured



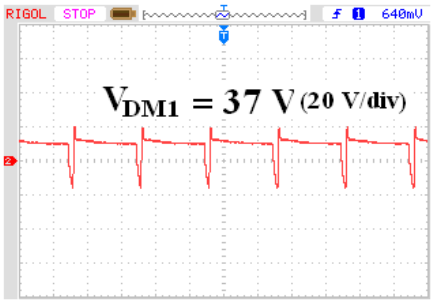

(a)




(b)

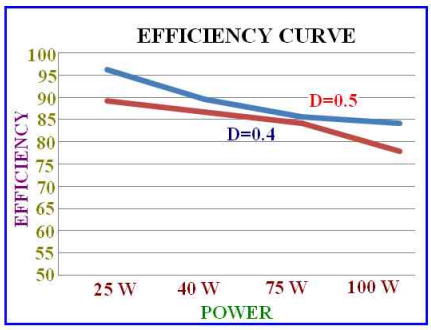



(c)




(d)


(e)




(f)

**Fig. 10** (a) Output Voltage and Switch Voltage for D= 0.34; (b) Output Voltage and Switch Voltage for D= 0.3; (c) Output Voltage and Switch Voltage for D=0.25; (d) Voltage Multiplier diode voltage ($D_{M1}$) and = $\frac{V_o}{M+1}$ = 37 V for D=0.34; (e) Photograph of the proposed –II topology; (f) Efficiency Vs output power for D= 0.4 &0.5.

**Table 5**: Comparison of output and switch voltage

| Duty Ratio | Theoretical | | Simulation | | Experimental | |
|---|---|---|---|---|---|---|
| | $V_o$ | $V_{SW}$ | $V_o$ | $V_{SW}$ | $V_o$ | $V_{SW}$ |
| 0.34 | 73.8 | 36.9 | 73.5 | 38.9 | 72 | 37 |
| 0.3 | 63.67 | 31.8 | 63.5 | 33.4 | 62 | 34 |
| 0.25 | 53.3 | 26.6 | 53.1 | 28.1 | 52 | 28.8 |

**Table 6:** Efficiency comparison

| $P_O = 40$ W, $V_g = 12$ V, $D = 0.5$, $V_O$=144 V | | | | |
|---|---|---|---|---|
| Parameter | Superlift [29] | SH-SLC [30] | Converter with D-C-L Unit [7] | Proposed Type-II QBSLVM |
| Diode Loss | 5.826 | 2.4589 | 2.33 | 2.523 |
| Inductor Loss | 2.217 | 2.217 | 2.17 | 1.184 |
| Switch Loss | 0.5091 | 0.1299 | 0.4539 | 0.8650 |
| Capacitor Loss | 0.2586 | 0.2586 | 0.125 | 0.234 |
| Total Loss | 8.8107 | 5.0644 | 5.08 | 4.80 |
| Efficiency | 82 % | 88.7% | 88% | 89.3% |

efficiency is found to be 89%. Inductor loss is considered to be lesser as compared to other converters made for comparison. About 7% efficiency improvement is observed in the proposed type-II topology over the Superlift converter.

This topology is best suited for fuel cell application because of continuous and ripples free input current. All the hardware results are obtained from a RIGOL DS1052E/50 MHz Digital storage oscilloscope. Hardware results almost match with simulation waveforms shown in Fig. 9(a)-(d). The voltage waveforms match with the derived formulae and steady state analysis of the proposed type-II converter.

Table 5 gives the theoretical, simulation and experimental comparison of the output voltage and voltage stress across the switch for different duty cycle. An experimental result closely matches with the simulated and theoretical results and the type-II converter performance is validated with this outcome. Fig. 10(f) gives the efficiency versus output power for two different duty cycles 0.4 and 0. 5. We infer that the proposed converters are suitable for low power application like automotive headlamps. The nominal power rating of automotive headlamps with HID lamps is 35-40 W.

## 7. Conclusion

In this paper, two non-isolated converters based on switched inductor and voltage multiplier cell has been derived and studied. The detailed analysis of proposed type-I converter is carried out in CCM and DCM mode. We analyzed the type-II converter in continuous conduction mode. The various parameters of type-I and II are compared with other converters in literature. Finally, a 40-W prototype circuit of the proposed type-II converter is designed to validate the result due to its superiority compared to type-I. The following are the characteristics of the proposed converter:

1) The voltage gain is high, and it is possible to attain a voltage gain of twelve with the duty cycle of 0.5 with type- II topology.
2) Due to the integration of SL and VM cell, the proposed converter has less current and voltage stress on power semiconductor devices. Thus, it allows us to select switch with low $R_{DS(on)}$ and thereby alleviating the switch conduction loss.
3) Total device count of the proposed converters is less for high voltage gain.
4) Efficiency of the proposed type-II topology is high compared to other converters taken for comparison

It can also be concluded that the proposed converter is much suitable for low power applications like high-intensity discharge lamp, where a high voltage is required for steady-state operation of the lamp.

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**Divya Navamani. J** She received the B. E. degree from Madras University and the M. E. degree from Sathyabama University in power electronics and Industrial drives. She is currently working in the area of Industrial drives. Her research interests include power electronics, electric and hybrid electric vehicle DC-DC converter. She is the life member of IEI, ISTE. She is also an annual member of IEEE.

**K. Vijayakumar** He received the B. E and M. E degree from Annamalai University in Power systems. His research interests include Power system: Deregulation, Modeling, Control and Operation, Optimization, FACTS, Power Quality. He is a life member of IEI, ISTE. He is also an annual member of IEEE.

**R. Jegatheesan** He received the B. E degree from Madras University and Msc (Engg) in Power systems from Madras University. He completed his Ph. D in the year 1975 from IIT, Kanpur. His research interests include large scale, Power system, power system optimization and state Estimation. He is a life member of ISTE. He is also an annual member of IEEE.

**Lavanya. A** She received the B. E. degree from Madras University and the M. E. degree from Sathyabama University in power electronics and Industrial drives. She is currently working in the area of Industrial drives. Her research interests include DC-DC converter, soft switching, fuzzy and neural network. She is the life member of IEI, ISTE. She is also an annual member of IEEE.