Single Input Multi Output DC/DC Converter: An Approach to Voltage Balancing in Multilevel Inverter

M. R. Banaei†, B. Nayeri* and E. Salary*

Abstract – This paper presents a new DC/AC multilevel converter. This configuration uses single DC sources. The proposed converter has two stages. The first stage is a DC/DC converter that can produce several DC-links in the output. The DC/DC converter is one type of boost converter and uses single inductor. The second stage is a multilevel inverter with several capacitor links. In this paper, one single input multi output DC-DC converter is used in order to voltage balancing on multilevel converter. In addition, as compare to traditional multilevel inverter, presented DC/AC multilevel converter has less on-state voltage drop and conduction losses. Finally, in order to verify the theoretical issues, simulation and experimental results are presented.

Keywords: DC-DC converter, Single input multi output, Voltage balancing

1. Introduction

Multilevel voltage source inverters provide a cost effective solution in the medium and high voltage systems. These converters have been widely applied to power generation, energy transmission, drives and power quality devices [1-5]. Nowadays, there exist different commercial topologies of multilevel voltage source inverters. The famous types of multilevel voltage source inverters are: neutral point clamped (NPC), flying capacitors (FC) and cascaded H-bridge (CHB) [3-6]. In comparison with the two-level have some advantages as:

- production of high power quality waveforms
- production of waveforms with lower harmonic components
- using lower voltage ratings of devices
- lower switching losses
- reduction of \( \frac{dv}{dt} \) stresses on the load
- the possibility of working with low speed semiconductors

The main disadvantage associated with the multilevel configurations is their circuit complexity, requiring a high number of power switches; they also require a great number of DC sources, provided either by independent supplies or, more commonly, by a cumbersome array of capacitive voltage dividers. Recently, several multilevel inverter topologies have been developed for multilevel inverters.

Novel topologies of multilevel inverters using a reduced number of switches, gate driver circuits and DC sources are presented in recent years [7-10]. In [7] and [8] novel configuration of multilevel inverters have been proposed. The suggested topologies need fewer switches and gate driver circuits. The proposed structure in [7] requires multiple DC sources. The converter power stage under study in [8] consists of an H-Bridge, bidirectional auxiliary switches, and an \( n \)-level capacitor voltage divider. In this case, ensuring that the DC voltages are kept in equilibrium is another factor that increases the complexity of the circuit.

Recently cascaded transformer multilevel topology is proposed [9, 10]. This has the advantage of having single DC source for all its cells. These topologies use transformers in their structures. However, transformers have some disadvantages such as heavy weight, large size, sensitivity to harmonics, voltage drop under load, requiring protection from system disturbances and overload, and environmental concerns regarding mineral oil [11, 12].

In recent years, significant advances in power semiconductor device technology have led to a number of multistage power converter topologies. A new type of converter based on power electronics has been introduced [13, 14].

This paper presents a new topology of multilevel inverter that improves the previous topologies and enhances its performance. This converter is a two stage converter. In the proposed topology, one type of multilevel inverter and one type of DC-DC converter have been integrated to reduce the number of switches and DC sources. The DC-DC converter is a multi-output boost converter. This configuration can be utilized instead of several single output DC power supplies. One type of multilevel inverter with a small number of switching devices is used in the second stage of converter. It consists of an H-bridge and an inverter which outputs multilevel voltage by switching the DC voltage sources in series. The proposed topology is called SIBMI (Single input boost multilevel inverter). To verify the feasibility of the proposed multilevel inverter;
we carried out computer-aided simulations using MATLAB / SIMULINK and experimental results.

2. Proposed SIBMI Topology

In Fig. 1, the proposed topology is shown in block diagram form. As can be seen, it is a two stage converter. In the input stage, the primary voltage is divided equally between the input stage modules. The DC outputs of the proposed DC-DC converter modules connected in series to supply the output stage. The output stage converts the resulting bipolar voltage DC into staircase AC voltage. A circuit diagram of the SIBMI is shown in Fig. 2. This circuit consists of switches, diodes, an inductor and capacitors.

2.1. Input stage

The input stage of the SIBMI is directly connected with the primary source. By controlling the switches of proposed DC-DC converter, the DC link capacitors can be regulated to the desired voltage level. To show the operation of input stage a simple case has been selected. Fig. 3 shows the one type of boost DC-DC converter that is connected to two loads (R1 and R2).

To analyze the steady-state performance of the converter, following parameters are supposed as:

T: switching period
D0: duty cycle of S0
D1: duty cycle of S1
Vo2>Vo1

Based on the switching states of S0 and S1 this configuration operates in three different states. Fig. 4 illustrates the equivalent power circuit in the three states.

As depicted during the first stage when S0 is turned “on”, the diodes block the charging current through capacitor as the voltage across the diode will be negative. The incremental current of inductor can be obtained as:

\[ \Delta I_1 = \frac{V_{o2} D_1 T}{L} \] (1)

The inductor current decreases during state 2 and 3. The decrease in inductor current in these states can be obtained as:

\[ \Delta I_2 = \frac{(V_{o1} - V_{o2})(D_1 - D_0) T}{L} \] (2)
\[ \Delta I_3 = \frac{(V_{o2} - V_{o1})(1 - D_1) T}{L} \] (3)

At steady state the increase in inductor current is equal to the decrease in inductor current. The average inductor voltage over one cycle should be zero in the steady state.

\[ \Delta I_1 = \Delta I_2 + \Delta I_3 \] (4)
\[ V_o = V_{o1}(D_1 - D_0) + V_{o2}(1 - D_1) \] (5)
Also, the average capacitor current over one cycle should be zero in the steady state.

\[ D_0 T \left( \frac{V_{o1}}{R_1} \right) + (D_1 - D_0) T \left( I - \frac{V_{o1}}{R_1} \right) + (1 - D_1) T \left( -\frac{V_{o1}}{R_1} \right) = 0 \]

\[ I = \frac{V_{o1}}{R_1 (D_1 - D_0)} \]  \hspace{1cm} (6)

\[ D_0 T \left( \frac{V_{o2}}{R_2} \right) + (D_1 - D_0) T \left( -\frac{V_{o2}}{R_2} \right) + (1 - D_1) T \left( I - \frac{V_{o2}}{R_2} \right) = 0 \]

\[ I = \frac{V_{o2}}{R_2 (1 - D_1)} \]  \hspace{1cm} (7)

From (5) to (7), the steady-state equation of output voltage can be derived as follows:

\[ V_{o1} = \frac{R_1 (D_1 - D_0) V_\text{in}}{R_1 (D_1 - D_0)^2 + R_1 (D_1 - D_0) + R_c (D_1 - D_0)^2} \]  \hspace{1cm} (8)

\[ V_{o2} = \frac{R_1 (1 - D_1) V_\text{in}}{R_1 (1 - D_1)^2 + R_c (D_1 - D_0)^2} \]  \hspace{1cm} (9)

2.2. Output stage

This inverter has two parts: main switches (basic unit) and one H-bridge cell. The basic unit produces waveform with one polarity in two half period. Operation of basic unit is the same as electrical tap changer. Fig. 5 shows circuit diagram of output stage and operation of basic unit as voltage selector. By changing the place of selector different voltage of DC sources are selected and different levels are generated. H-bridge cell inverses waveform in half period and produces zero level. So other polarity of waveform is obtained and sinusoidal waveform is produced. Zero level could be produced with H1 and H3 or H2 and H4.

There are several modulation strategies for multilevel inverters. In this work, the fundamental frequency switching technique has been used [15]. The control of the new family of multilevel inverters is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform.

With suitable toggling of switches, a phase voltage waveform is obtained. The effective number of output voltage levels is given by (10).

\[ m = 2n + 1 \]  \hspace{1cm} (10)

\( n \) is number of DC voltage sources. The maximum output voltage \( V_\text{OMax} \) can be determined by:

\[ V_{\text{Omax}} = V_\text{in} + V_{c1} + V_{c2} + \ldots + V_{cn} \]  \hspace{1cm} (11)

3. Simulation Results

To examine the performance of the proposed multistage converter in the generation of a desired output AC voltage waveform, a prototype is simulated and implemented based on the proposed topology according to that one shown in Fig. 6. The MATLAB software has been used for simulation. The converter shown in Fig. 6 is a 9-level multilevel inverter and can generate staircase waveform.

<table>
<thead>
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<th>Table 1. Parameters of simulation.</th>
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<tr>
<td><strong>Parameters</strong></td>
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<tr>
<td>Input line voltage</td>
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<tr>
<td>L, C (DC-DC converter)</td>
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<tr>
<td>Input switching frequency</td>
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<td>Load</td>
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The parameters of simulation have shown in Table 1.

In the 4-output DC–DC converter, there are four possible switching states. $S_1$, $S_2$ and $D_1$ cannot be turned ‘on’ while $S_0$ is ‘on’. The operation principle of this approach will be similar to boost converter.

As shown in Fig. 7, the boost input converter consists of inductor $L$, diodes $D_1$, $D_2$, $D_3$, switches $S_0$, $S_1$, $S_2$ and output capacitors $C_1$, $C_2$, $C_3$. When the switch $S_0$ turns on, the diodes and other switches turn off. The current flows through inductor $L$ and switch $S_0$. Therefore, the amount of inductor current increases linearly. When the switch $S_0$ turns off, the switch $S_1$ turns on and the current flows through inductor $L$ and capacitor $C_1$. Hence, the amount of inductor current decreases. When the voltage of capacitor $C_1$ reaches to desired value then the switch $S_1$ is turned off and the switch $S_2$ is turned on.

When the voltage of capacitor $C_2$ reaches to desired value then the switch $S_2$ is turned off and the diode $D_3$ is turned on. The amount of inductor current decreases linearly in these steps. To regulate capacitors voltage at desired value, a simple control method is used. The block diagram of capacitors voltage regulator is shown in Fig. 7(b). Fig. 8 shows operation of input stage.

The output stage is multilevel inverter. Fig. 9 shows
operation of output stage. The output voltage \( V_o \) is a 50 Hz staircase waveform with amplitude 40 V. As it can be seen, the results verify the ability of proposed inverter in generation of desired output voltage waveform.

4. Experimental Results

To show the performance of the proposed converter, experimental results have been performed. In this test \( L \), \( C1=C2=C3=220 \mu F \), \( V_{in}=10 \) V. MOSFET IRFP450 is used as the switching devices and RHRG3060C is used as the diodes. The gate driving signal is given by Atmega 32 microcontroller and TLP250.

Fig. 10 shows the measured waveforms. Figs. 10(a) and 10(b) show the measured results of input inductor voltage and current. Fig. 10(c) shows the measured output voltage.

Fig. 10. The measured waveforms: (a) Measured inductor voltage; (b) Measured inductor current (voltage of 2.5Ω resistance); (c) Measured output voltage.

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5. Conclusions

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References

Ebrahim Salary was born in Khoram Abad, Iran, in 1981. He received his B.S. Degree in Power Electrical Engineering from Dezful Azad University, Dezful, Iran, in 2004. He received his M.S. degree from Tarbiat Moallem University of Azarbaijan, Tabriz, Iran, in 2010. He is currently a Ph.D. student at the Electrical Engineering Department of Azarbaijan Shahid Madani University, Iran. His main research interests include power electronics, power quality, energy conversion and renewable energy.