Analysis of an Interleaved Resonant Converter for High Voltage and High Current Applications

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Abstract – This paper presents an interleaved resonant converter to reduce the voltage stress of power MOSFETs and achieve high circuit efficiency. Two half-bridge converters are connected in series at high voltage side to limit MOSFETs at $V_{in}/2$ voltage stress. Flying capacitor is used between two series half-bridge converters to balance two input capacitor voltages in each switching cycle. Variable switching frequency scheme is used to control the output voltage. The resonant circuit is operated at the inductive load. Thus, the input current of the resonant circuit is lagging to the fundamental input voltage. Power MOSFETs can be turn on under zero voltage switching. Two resonant circuits are connected in parallel to reduce the current stress of transformer windings and rectifier diodes at low voltage side. Interleaved pulse-width modulation is adopted to decrease the output ripple current. Finally, experiments are presented to demonstrate the performance of the proposed converter.

Keywords: Flying capacitor, DC converter.

1. Introduction

Power converters for medium or high power applications have been proposed and applied for many industry applications, such as fuel-cell power system [1], charge system [2] and ship power system [3]. For three-phase AC/DC power conversion systems, the front stage is a power factor corrector (PFC) and the second stage a DC/DC converter. The DC bus voltage of a three-phase PFC may be equal to 800V. In DC/DC converter, power MOSFETs with 900V voltage stress will result in high turn-on resistance. Three-level converters [4-9] with low voltage stress and high switching frequency have been presented in DC/DC converters for high voltage applications. Based on the neutral-point clamped diodes or flying capacitor, the voltage stress of active switches is clamped at $V_{in}/2$. However, two input split capacitor voltages maybe unbalanced and will increase the voltage stress of active switches beyond $V_{in}/2$. In [1] and [10], flying capacitor is adopted to the conventional three-level neutral point clamped converter to automatically balance two input capacitor voltages. Three-level zero voltage switching (ZVS) converters [11-17] have been presented to reduce the switching losses and increase the circuit efficiency. Pulse-width modulation (PWM) schemes are adopted to generate the PWM signals for active switches and to regulate output voltage. However, the ZVS condition of active switches is related to the load condition and input voltage so that it is difficult to implement ZVS turn-on for all switches over the entire load range. In order to extend the ZVS condition over the whole load range, resonant converters [18-22] have been proposed to achieve ZVS turn-on over the wide load range and input voltage variation. However, the ripple current at the output capacitor in resonant converter is higher than the output ripple current in the conventional half-bridge or full-bridge PWM converter. In order to limit the output ripple voltage in the desired ripple voltage specification, several capacitors are connected in parallel to reduce the resultant series equivalent resistance. Therefore, the large capacitance is normally adopted at the output side in the resonant converters. In order to reduce the output capacitance and output ripple current in the resonant converters, parallel resonant converter with interleaved PWM scheme has been presented in [23-25].

A new parallel resonant converter is presented for high input voltage and high load current applications. Two circuit modules connected in parallel in order to share load power and reduce the current stress of all passive and active power components. These two circuit modules are controlled with the phase shift of one-fourth switching period in order to reduce the ripple current at the output capacitor. Thus, the size of output capacitor can be reduced. In each circuit module, two half-bridge converters are connected in series at the primary side to reduce the voltage stress of each active switch at $V_{in}/2$. Flying capacitor is connected between two half-bridge converters such that two input capacitor voltages can be automatically balanced in each switching cycle. Series-parallel resonant tank is adopted in each half-bridge converter to achieve ZVS turn-on for all switches over the entire load range. Finally, experiments were provided to verify the performance of the proposed converter.

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2. Circuit Configuration

Fig. 1 gives the circuit configuration of the proposed converter for three-phase switching mode power supplies. The three-phase AC/DC converter with power factor correction is used in the front stage to reduce line current harmonics and provide a stable DC bus voltage for second stage DC/DC converter. The DC bus voltage is about 750V-800V for three-phase 480V utility input with power factor correction. The proposed parallel DC/DC converter with low voltage stress MOSFETs is adopted in the second stage for high load current applications. Two circuit modules are adopted in the proposed converter to share load current and reduce the current rating of active and passive components. The first circuit module includes $C_{in1} - C_{in2}$, $C_{f1}$, $S_1 - S_8$, $C_{S1} - C_{S6}$, $L_{r1} - L_{r6}$, $T_1 - T_2, D_1 - D_4$ and $C_o$. In the same manner, the components of $C_{in1} - C_{in2}$, $C_{f2}$, $S_1 - S_8$, $C_{S1} - C_{S6}$, $L_{r1} - L_{r6}$, $T_1 - T_2, D_1 - D_4$ and $C_o$ are included in the circuit module 2. $C_{in1}$ and $C_{in2}$ are two input capacitances. $C_{f1} - C_{f2}$ are the series resonant capacitances. $L_{r1} - L_{r6}$ are the series resonant inductances. $L_{m1} - L_{m4}$ are the magnetizing inductances of transformers $T_1 - T_2$, respectively. $D_1 - D_4$ are the rectifier diodes and $T_1 - T_4$ are the isolated transformers. $C_{f1}$ and $C_{f2}$ are the flying capacitances. Each circuit module includes two resonant converters with half-bridge converter leg. In circuit module 1, the first resonant converter includes the components of $S_1, S_2, C_{r1}, L_{r1}, T_1, D_1, D_2$ and $C_o$. The second resonant converter includes $S_3, S_4, C_{r2}, L_{r2}, T_2, D_3$ and $C_o$. $C_o$ is the output capacitance. The primary sides of two resonant converters are connected in series in order to limit the voltage stress of each active switch at $V_{in}/2$. Active switches $S_1$ and $S_4$ have the same PWM signals. However, the PWM waveforms of $S_1$ and $S_2$ are complementary each other to avoid the short circuit in each half-bridge leg. In order to balance two input capacitor voltages $v_{Cin1}$ and $v_{Cin2}$, $C_{f1}$ is connected between the AC terminals $b$ and $c$ and $C_{f2}$ is connected between the AC terminals $f$ and $g$. If $S_1$ and $S_2$ are in the on-state and $S_3$ and $S_4$ are in the off-state, then $v_{Cf1}$= $v_{Cin1}$. On the other hand, $v_{Cf2}$= $v_{Cin2}$ if $S_3$ and $S_4$ are in the on-state. Since each active switch has the equal turn-on time, the flying capacitor voltage can be derived as $v_{Cf1}$=$v_{Cf2}$=$v_{Cin1}$=$v_{Cin2}$=$V_{in}/2$ and two capacitor voltages $v_{Cin1}$ and $v_{Cin2}$ are automatically balanced in each switching cycle. The frequency modulation scheme is used to regulate output voltage $V_o$. If the operated switching frequency is lower than the series resonant frequency, active switches $S_1 - S_4$ are turned on at ZVS and rectifier diodes $D_1 - D_4$ are turned off at ZCS. Thus, the switching losses of active switches are reduced and the reverse recovery problem of rectifier diodes is improved. In the proposed converter, each resonant converter supplies one-fourth of load.

![Fig. 1. Circuit configuration of the proposed converter with two circuit modules.](image1)

![Fig. 2. Key waveforms of the proposed converter.](image2)
power to output load for the medium/high load current applications.

3. Operation Principle

The circuit operations of the proposed converter are discussed with the following assumptions to simplify the system analysis. (1) Transformers $T_1 - T_4$ are identical with the same turns ratio $n_p/n_s = n_o/n_{s1}$ and same magnetizing inductances $L_{m1} = L_{m2} = L_{m3} = L_{m4} = L_m$. (2) $S_1 - S_5$ have the same output capacitance $C_o$. (3) $C_{in1} = C_{in2}$. (4) $C_r = C_{s1}$ and $C_r = C_{s2}$ and (5) $L_r = L_{r1} = L_{r2} = L_{r3} = L_r$. The main PWM waveforms of the proposed converter during one switching cycle are given in Fig. 2. Due to the on/off conditions of switches $S_1 - S_5$ and rectifier diodes $D_1 - D_4$, the proposed converter has twelve operation modes in one switching period. The corresponding equivalent circuits of twelve operation modes are shown in Fig. 3. Before time $t_0$, $S_1 - S_5$ are all turned off in circuit module 1. $i_{Lr1}$ and $i_{Lr2}$ are positive and negative, respectively. Therefore, $C_{r1}$ and $C_{r2}$ are charged. Since $i_{Lr1} < i_{Lm1}$ and $i_{Lr2} < i_{Lm2}$, diodes $D_7$ and $D_8$ are in the on-state. In circuit module 2, $S_5$ and $S_6$ are in the on-state and diodes $D_3$ and $D_4$ are conducting. $L_{r1}$ and $C_{r3}$ are resonant with the applied voltage $V_{in}/2 - nV_o - V_{o2}$, and $L_{r4}$ and $C_{r4}$ are resonant with the applied voltage $nV_o - V_{o2}$. Mode 1: ($t < t_0$): At $t_0$, capacitances $C_{r1}$ and $C_{r2}$ are discharged to zero voltage in circuit module 1. Since $i_{Lr1}$ and $i_{Lr2}$ are positive and negative, respectively, the anti-parallel diodes of $S_1$ and $S_2$ are conducting. Therefore, $S_1$ and $S_2$ can be turned on at this moment to achieve ZVS. In this mode, $i_{Lr1} < i_{Lm1}$ and $i_{Lr2} < i_{Lm2}$. Thus, $D_2$ and $D_3$ are conducting and the magnetizing voltages $V_{m1} = -nV_o$ and $V_{m2} = nV_o$. The magnetizing current $i_{Lm1}$ decreases with the slope of $-nV_o/L_m$ and $i_{Lm2}$ increases with the slope of $nV_o/L_m$. In module 1, $L_{r1}$ and $C_{r1}$ are resonant with the applied voltage $V_{in}/2 - nV_o - V_{o2}$, and the flying capacitor voltage $V_{o2} = v_{Cin1}$. In module 2, $S_5$ and $S_6$ are turned on and $D_3$ and $D_4$ are in the on-state. $L_{r3}$ and $C_{r3}$ are resonant with the applied voltage $V_{in}/2 - nV_o - V_{o2}$, and the flying capacitor voltage $V_{o2} = v_{Cin1}$. The inductor currents $i_{Lr1} - i_{Lr4}$ and capacitor voltages $v_{Cin1} - v_{Cin2}$ in this mode are given as:

$$i_{Lr1}(t) = \frac{nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr1}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr2}(t) = \frac{V_{in}/2 - nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr2}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr3}(t) = \frac{V_{in}/2 - nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr3}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr4}(t) = \frac{nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr4}(t_0) \cos \omega_r(t - t_0)$$

$$v_{Cin1}(t) = nV_o - [nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr1}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$v_{Cin2}(t) = v_{in}/2 - [V_{in}/2 - nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr2}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$= v_{in}/2 - nV_o - V_{o2}$$

$$v_{Cin1}(t) = nV_o - [nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr4}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$= v_{in}/2 - nV_o - V_{o2}$$

Mode 2 ($t < t_0$): At $t_0$, $S_1$ and $S_2$ are turned off in circuit module 1. Thus, $D_3$ and $D_4$ are in the off-state. Since $S_3$ and $S_4$ are still in the on-state, $C_{r3}$, $L_{r3}$, and $L_{r4}$ are resonant with the applied voltage $V_{in}/2 - V_{o2}$. In circuit module 2. The inductor currents $i_{Lr3}$ and $i_{Lr4}$ decrease and $i_{Lr2}$ and $i_{Lr3}$ increase in this mode.

Mode 3 ($t < t_0$): At $t_0$, $S_3$ and $S_4$ are turned off. Since $i_{Lr3}(t_0)$ and $i_{Lr4}(t_0)$ are positive and negative, respectively, the anti-parallel diodes of $S_3$ and $S_4$ are conducting. Therefore, $S_3$ and $S_4$ are turned on and $D_3$ and $D_4$ are in the on-state. $L_{r3}$ and $C_{r3}$ are resonant with the applied voltage $V_{in}/2 - nV_o = v_{Cin2}$, and the flying capacitor voltage $V_{o2} = v_{Cin2}$. The inductor currents $i_{Lr1} - i_{Lr4}$ and capacitor voltages $v_{Cin1} - v_{Cin2}$ in this mode are given as:

$$i_{Lr1}(t) = \frac{nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr1}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr2}(t) = \frac{V_{in}/2 - nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr2}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr3}(t) = \frac{V_{in}/2 - nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr3}(t_0) \cos \omega_r(t - t_0)$$

$$i_{Lr4}(t) = \frac{nV_o - v_{Cin2}(t)}{Z_r} \sin \omega_r(t - t_0)$$

$$+ i_{Lr4}(t_0) \cos \omega_r(t - t_0)$$

$$v_{Cin1}(t) = nV_o - [nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr3}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$v_{Cin2}(t) = V_{in}/2 - [V_{in}/2 - nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr3}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$= v_{in}/2 - nV_o - V_{o2}$$

$$v_{Cin1}(t) = nV_o - [nV_o - v_{Cin2}(t)] \cos \omega_r(t - t_0)$$

$$+ i_{Lr4}(t_0) Z_r \sin \omega_r(t - t_0)$$

$$= v_{in}/2 - nV_o - V_{o2}$$
Fig. 3. Operation modes of the proposed converter during one switching cycle: (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10 (k) mode 11 (l) mode 12.
can be turned on at this moment to achieve ZVS. Diodes $D_a$ and $D_b$ are conducting so that $V_{lam}=v_{L_{in}}$ and $V_{lam}=v_{L_{out}}$. In circuit module 2, $L_{r}$ and $C_{r}$ are resonant with the applied voltage $v_{L_{in}}$ and $L_{in}$ and $C_{in}$ are resonant with the applied voltage $V_{in}/2$ and $V_{in}/2-v_{C_{in}}$. The inductor currents $i_{L_{r}}$ and $i_{L_{in}}$ and the capacitor voltages $v_{C_{r}}$ and $v_{C_{in}}$ are expressed as:

$$i_{L_{r}}(t) = \frac{nV_{o} - v_{C_{r}}(t)}{Z_{r}} \sin \omega_{r}(t - t_{j}) + i_{L_{r}}(t) \cos \omega_{r}(t - t_{j})$$  \hspace{1cm} (13)$$

$$i_{L_{in}}(t) = \frac{V_{in}/2 - nV_{o} - v_{C_{r}}(t)}{Z_{r}} \sin \omega_{r}(t - t_{j}) + i_{L_{in}}(t) \cos \omega_{r}(t - t_{j})$$  \hspace{1cm} (14)$$

$$v_{C_{r}}(t) = nV_{o} - [nV_{o} - v_{C_{r}}(t)] \cos \omega_{r}(t - t_{j}) + i_{L_{r}}(t) Z_{r} \sin \omega_{r}(t - t_{j})$$  \hspace{1cm} (15)$$

$$v_{C_{in}}(t) = V_{in}/2 - nV_{o} - [V_{in}/2 - nV_{o} - v_{C_{in}}(t)] \cos \omega_{r}(t - t_{j}) + i_{L_{in}}(t) Z_{r} \sin \omega_{r}(t - t_{j})$$  \hspace{1cm} (16)$$

**Mode 5** [$t_{j} \leq t < t_{j+2}$]: At $t_j$, $i_{L_{in}}=i_{L_{r}}$ and $i_{L_{in}}=i_{L_{r}}$. Thus, $D_1$ and $D_2$ are turned off. Components $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $v_{C_{r}}(t)$ and $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $V_{in}/2-v_{C_{in}}(t)$. The inductor currents $i_{L_{r}}$ and $i_{L_{in}}$, and the capacitor voltages $v_{C_{r}}$ and $v_{C_{in}}$ are given as:

$$i_{L_{r}}(t) = \frac{-v_{C_{r}}(t)}{Z_{r}} \sin \omega_{r}(t - t_{j}) + i_{L_{r}}(t) \cos \omega_{r}(t - t_{j})$$  \hspace{1cm} (17)$$

$$i_{L_{in}}(t) = \frac{V_{in}/2 - v_{C_{in}}(t)}{Z_{r}} \sin \omega_{r}(t - t_{j}) + i_{L_{in}}(t) \cos \omega_{r}(t - t_{j})$$  \hspace{1cm} (18)$$

$$v_{C_{r}}(t) = v_{C_{r}}(t) \cos \omega_{r}(t - t_{j}) + i_{L_{r}}(t) Z_{r} \sin \omega_{r}(t - t_{j})$$  \hspace{1cm} (19)$$

$$v_{C_{in}}(t) = V_{in}/2 - [V_{in}/2 - v_{C_{in}}(t)] \cos \omega_{r}(t - t_{j}) + i_{L_{in}}(t) Z_{r} \sin \omega_{r}(t - t_{j})$$  \hspace{1cm} (20)$$

**Mode 6** [$t_{j+2} \leq t < t_{j+4}$]: At $t_{j+2}$, $S_1$ and $S_3$ are turned off and $D_1$ and $D_3$ are conducting. The magnetizing voltages $v_{L_{in}}=-nV_o$ and $v_{L_{out}}=-nV_o$. Since $i_{L_{r}}(t)<0$ and $i_{L_{in}}(t)=0$, $C_{r}$ and $C_{r}$ are charged and $C_{r}$ and $C_{r}$ are discharged. $C_{r}$ and $C_{r}$ can be discharged to zero voltage if the energy stored in $L_{r}$ and $L_{in}$ is greater than the stored energy in $C_{r}$ and $C_{r}$. At $t_{j+4}$, $v_{C_{r}}=v_{C_{in}}=0$. The anti-parallel diodes of $S_1$ and $S_3$ are conducting.

**Mode 7** [$t_{j+4} \leq t < t_{j+6}$]: At $t_{j+4}$, $C_{r}$ and $C_{r}$ are discharged to zero voltage in circuit module 1. Since $i_{L_{r}}(t)<0$ and $i_{L_{in}}(t)=0$, the anti-parallel diodes of $S_1$ and $S_3$ are conducting. Thus, $S_1$ and $S_3$ can be turned on at this moment to achieve ZVS. In module 1, $L_{r}$ and $C_{r}$ are resonant with the applied voltage $V_{in}/2-nV_o-v_{C_{r}}(t)$, $L_{in}$ and $C_{in}$ are resonant with the applied voltage $nV_o-v_{C_{in}}(t)$, and the flying capacitor voltage $v_{C_{f}}=v_{C_{in}}$. The operation of circuit module 2 in this mode is the same as the operation in the previous mode.

**Mode 8** [$t_{j+6} \leq t < t_{j+8}$]: At $t_{j+6}$, $i_{L_{r}}(t)=i_{L_{in}}$ and $i_{L_{in}}(t)=i_{L_{in}}$. Thus, $D_3$ and $D_6$ are all turned off. In circuit module 2, $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $-v_{C_{r}}(t)$ and $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $V_{in}/2-v_{C_{in}}(t)$. The operations of circuit module 1 in this mode are the same as the operation in the previous mode.

**Mode 9** [$t_{j+8} \leq t < t_{j+10}$]: At $t_{j+8}$, $S_1$ and $S_3$ are turned off. Since $i_{L_{r}}(t)<0$ and $i_{L_{in}}(t)=0$, $C_{r}$ and $C_{r}$ are discharged and $C_{r}$ and $C_{r}$ are charged in this mode. Diodes $D_1$ and $D_3$ are conducting. $C_{r}$ and $C_{r}$ can be discharged to zero voltage if the energy stored in $L_{r}$ and $L_{in}$ is greater than the energy stored in $C_{r}$ and $C_{r}$. Therefore, the energy stored in $L_{r}$ and $L_{in}$ is greater than the energy stored in $C_{r}$ and $C_{r}$.

**Mode 10** [$t_{j+10} \leq t < t_{j+12}$]: At $t_{j+10}$, $i_{L_{r}}(t)=i_{L_{in}}$ and $i_{L_{in}}(t)=i_{L_{in}}$. Thus, $D_1$ and $D_3$ are all turned off. In circuit module 1, $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $V_{in}/2-nV_o-v_{C_{r}}(t)$ and $L_{in}$ and $C_{in}$ are resonant with the applied voltage $-v_{C_{r}}(t)$). The operation of circuit module 2 is the same as the operation in the previous mode.

**Mode 11** [$t_{j+12} \leq t < t_{j+14}$]: At $t_{j+12}$, $i_{L_{r}}(t)=i_{L_{in}}$ and $i_{L_{in}}(t)=i_{L_{in}}$. Thus, $D_1$ and $D_3$ are all turned off. In circuit module 1, $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $V_{in}/2-nV_o-v_{C_{r}}(t)$ and $C_{r}$, $L_{r}$ and $L_{in}$ are resonant with the applied voltage $-v_{C_{r}}(t)$). The operation of circuit module 2 is the same as the operation in the previous mode.

4. **System Analysis**

In this section, the system analysis of the proposed converter is presented. The duty cycle of each active switch is equal to 0.5. The pulse frequency modulation is adopted to regulate output voltage. The analysis of the proposed converter is based on the fundamental harmonic approach. The fundamental switching frequency is adopted to derive the system transfer function for each resonant converter. All harmonics of the switching frequency are neglected in the following discussion. The PWM signals of two circuit modules are interleaved by one-fourth of switching period. Each resonant circuit supplies one-fourth of load power to output load. Since the duty ratio of $S_1$ and $S_3$ is equal to 0.5, the AC terminal voltages $V_{d}$, $V_{d}$, and $V_{d}$ are the square waveforms between 0 and $V_{in}/2$. The capacitor voltage $v_{C_{f}}=v_{C_{in}}$ in modes 1-5 and $v_{C_{f}}=v_{C_{in}}$ in...
modes 7-11. The time periods in these two intervals are the same. Thus, the input capacitor voltages can be compensated and identical each other \( v_{cin1} = v_{cin2} \). Based on the Fourier series analysis, the AC terminal voltage \( v_{ab} \) can be expressed as:

\[
v_{ab} = \frac{V_{in}}{4} + \frac{V_{in}}{\pi} \sin(2nf_r t) + \sum_{n=3}^{\infty} \frac{V_{in}}{n\pi} \sin(2nfee t)
\]

\[
v_{ab} = v_{ab,c} + v_{ab,f} + v_{ab,h}
\]

where \( v_{ab,c} \), \( v_{ab,f} \) and \( v_{ab,h} \) are the dc component, fundamental frequency component and harmonic components of \( v_{ab} \), respectively. The secondary side of resonant converter is driven by a quasi-sinusoidal current. If \( L_r < L_{m1} \), \( D_s \) is conducting and the magnetizing voltage \( v_{Lm} = nV_o \). On the other hand, \( v_{Lm} = -nV_o \) if \( L_r < L_{m1} \) and \( D_s \) is conducting. The transformer primary voltage \( v_{Lm} \) can be considered as a quasi-square waveform with \( \pm nV_o \). The peak voltage of \( v_{Lm} \) at the fundamental frequency is expressed as \( \tilde{v}_{Lm1} = 4nV_o/\pi \). The average output current of each center-tapped rectifier is equal to \( I_o/4 \) and the peak value of diode currents is given as \( I_{o1,2} = \pi I_o/8 \). The load resistance reflected to the primary side of \( T_1 \) is given as \( R_{ac,T1} = \tilde{v}_{Lm1}/(I_{o1} / n) = 32n^2 R_o / \pi^2 \). Therefore, the resonant tank by \( L_{r1}, C_{r1} \) and \( L_{m1} \) is excited by an effectively sinusoidal input voltage \( V_{ab,f} \) and drives the effective AC resistive road \( R_{ac,T1} \). Thus, the AC voltage gain of the resonant tank by \( L_{r1}, C_{r1} \) and \( L_{m1} \) at fundamental frequency can be obtained as:

\[
|G_{ac}(f)| = \frac{V_{ac,f}}{V_{ab,f}} = 1/\left[ \frac{1}{1+k}(1-f_r^2/f_s^2) \right] + Q^2(f_s^2 - f_r^2/ f_r^2)
\]

where \( Q = \sqrt{L_{r1}/C_{r1} / R_{ac,T1}} \), \( f_s = 1/2\pi \sqrt{L_{r1}/C_{r1}} \), \( k=L_r/L_{m1} \) and \( f_r \) is the switching frequency. At no-load condition \( (Q=0) \) and \( f_s = \omega_c \), the AC voltage gain of each resonant converter is expressed as \( |G_{ac}(f)|_{Q=0, f_s=\omega_c} \approx 1/(1+k) \). If the minimum DC voltage gain of the resonant converter is greater than \( |G_{dc}(f)|_{Q=0, f_s=\omega_c} \), then the output voltage can be controlled from no load to full load condition.

5. Design Example and Experimental Results

A laboratory prototype was implemented with the following specifications: \( V_{in} = 750V \) \(-800V\), \( V_o = 24V \), \( I_o = 60A \), and resonant frequency \( f_s = 1200Hz \). Transformers \( T_1 \) \(-T_3 \) were implemented with TDK EER-42 magnetics core with \( A_m = 194mm^2 \). The primary and secondary winding turns of \( T_1 \) \(-T_4 \) are 48 turns and 6 turns, respectively. The minimum and maximum voltage gains of resonant converter are given as:

\[
G_{dc,min} = \frac{4n(V_o + V_f)}{V_i_{min}} = \frac{4 \times (48/6) \times (24 + 0.8)}{800} \approx 0.992
\]

\[
G_{dc,max} = \frac{4n(V_o + V_f)}{V_i_{max}} = \frac{4 \times (48/6) \times (24 + 0.8)}{750} = 1.058
\]

where \( V_f \) is the voltage drop on diodes \( D_1 \) \(-D_6 \). At full load, the AC equivalent resistances \( R_{ac,T1} \) \(-R_{ac,T4} \) are given as:

\[
R_{ac,T1} = R_{ac,T2} = R_{ac,T3} = R_{ac,T4} = 32 \times (48/6)^2 \times (24/60)/3.1416^2 = 83\Omega
\]

In this prototype, the inductance ratio \( k=L_r/L_{m1} \) is selected as \( 1/8 \) and the quality factor \( Q \) at full load is selected as 0.3. Thus, the AC voltage gain of the proposed converter at no load condition \( (Q=0) \) is obtained as \( |G_{ac}(f)|_{Q=0, f_s=\omega_c} \approx 0.889 \). In (23), the minimum DC voltage gain \( G_{dc,min} \) of the proposed converter is 0.992 and greater than the AC voltage gain at no load condition. Thus, the output voltage at no load condition can be controlled. From the given series resonant frequency \( f_s \), the selected quality factor \( Q \), the inductance ratio \( k \) and the AC equivalent resistance \( R_{ac,T1} \), the series resonant inductances \( L_{r1} \) \(-L_{r4} \), the magnetizing inductances \( L_{m1} \) \(-L_{m4} \) and the resonant capacitors \( C_{r1} \) \(-C_{r4} \) can be obtained as:

\[
L_{r1} = L_{r2} = L_{r3} = L_{r4} = \frac{QR_{ac,T1}}{2\pi f_s} = \frac{0.3 \times 83}{2\pi \times 120 \times 10^3} = 0.33\mu H
\]

\[
L_{m1} = L_{m2} = L_{m3} = L_{m4} = L_{r1}/k = \frac{33\mu H}{1/8} = 264\mu H
\]

\[
C_{r1} = C_{r2} = C_{r3} = C_{r4} = \frac{1}{4\pi^2 L_{r1}/f_s^2} = 53nF
\]

Since two flying capacitors \( C_{r1} \) and \( C_{r2} \) are used to balance two input capacitor voltages \( V_{cin1} \) and \( V_{cin2} \), the voltage stresses of \( S_1 \) \(-S_8 \) can be limited at \( V_{in,max}/2 \).

\[
v_{S1, stress} = V_{in,max}/2 = 400V
\]

The MOSFETS IRFP460 with 500V voltage stress and 20A current stress are adopted for active switches \( S_1 \) \(-S_8 \). The voltage stress and average current of rectifier diodes \( D_1 \) \(-D_8 \) are obtained as:

\[
v_{D1, stress} = 2(V_o + V_f) = 2 \times (24 + 0.8) = 49.6V
\]

\[
l_{D1, ave} = l_{max}/8 = 60/8 = 7.5A
\]

The fast recovery diodes 30CPQ150 with 150V voltage stress, 30A current stress and 0.8V voltage drop are used for diodes \( D_1 \) \(-D_6 \). The input capacitances \( C_{in1} \) and \( C_{in2} \) are 680nF/450V, the flying capacitances \( C_{r1} \) and \( C_{r2} \) are 680nF/630V, and the output capacitance \( C_o \) is 2820\mu F/100V (6 \times 470\mu F/100V).
A laboratory prototype with the circuit parameters derived in the previous section was implemented and tested to verify the effectiveness of the proposed converter. The measured gate voltages of $S_1$–$S_8$ with input voltage $V_{in}=800$V and 25% load and full load are shown in Fig. 4. The PWM signals of $S_1$–$S_4$ are phase-shifted one-fourth of switching period with respectively to PWM signals of $S_5$–$S_8$, respectively. Fig. 5 gives the measured results of gate voltage, drain voltage and drain current of switch $S_1$ at 5% load with different input voltage cases. Before switch $S_1$ is turned on, the drain current is negative to discharge the drain-to-source capacitor. Thus, switch $S_1$ can be turned on.

![Fig. 4. Measured waveforms of the gate voltages $v_{S1,gs}$–$v_{S8,gs}$ with $V_{in}=800$V and (a) 25% load (b) full load.](image)

![Fig. 5. Experimental results of gate voltage, drain voltage and drain current of switch $S_1$ at 5% load with (a) $V_{in}=750$V (b) $V_{in}=800$V.](image)

![Fig. 6. Experimental results of gate voltage, drain voltage and drain current of switch $S_1$ at full load with (a) $V_{in}=750$V (b) $V_{in}=800$V.](image)

![Fig. 7. Measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and $V_{in}=800$V.](image)
on under ZVS when drain voltage is decreased to zero voltage. In the same manner, Fig. 6 shows the measured gate voltage, drain voltage and drain current of $S_1$ at full load and different input voltage conditions. From measured results shown in Figs. 5 and 6, $S_1$ is turned on at ZVS from 5% load to full load. Similarly, $S_2$ to $S_8$ can also be turned on under ZVS from 5% load to full load. Fig. 7 illustrates the measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and $V_{in}=800V$. Two input capacitor voltages and two flying capacitor voltages are all balanced at 400V. Fig. 8 gives the measured waveforms of inductor currents $i_{Lr1}$ to $i_{Lr4}$ at full load. Four inductor currents $i_{Lr1}$ to $i_{Lr4}$ are balanced. Fig. 9

Fig. 8. Measured waveforms of inductor currents $i_{Lr1}$ to $i_{Lr4}$ at full load with (a) $V_{in}=750V$ (b) $V_{in}=800V$.

Fig. 9. Measured waveforms of resonant capacitor voltages $v_{Cr1}$ to $v_{Cr4}$ at full load with (a) $V_{in}=750V$ (b) $V_{in}=800V$.

Fig. 10. Measured waveforms of the center-tapped rectifier output currents $i_{o1}$ to $i_{o4}$ at full load with (a) $V_{in}=750V$ (b) $V_{in}=800V$.

Fig. 11. Measured efficiencies of the proposed converter at different input voltage and load current conditions.
shows the measured waveforms of four resonant capacitor voltages \( v_{Cr1} - v_{Cr4} \) at full load condition. Fig. 10 gives the test results of the rectifier output currents \( io1 - io4 \) at full load condition. The rectifier output currents \( io1 - io4 \) are almost balanced. It is clear that output currents \( io1 \) and \( io4 \) are phase-shifted one-half of switching cycle with respect to \( io2 \) and \( io3 \). The ripple current of \( io2 \) is about 30A. However, the ripple current of the resultant output current \( io1 + io2 + io3 + io4 \) is about 10A. The measured output ripple voltage is 2.1V at full load. Fig. 11 shows the measured circuit efficiencies of the proposed converter at different input voltage and load current conditions.

6. Conclusion

A new parallel resonant converter is presented for high input voltage and high load current applications. The main functions of the proposed converter are low voltage stress of MOSFETs, ZVS turn-on for all MOSFETs, no reverse recovery loss on rectifier diodes, low current rating of transformer windings and less ripple current on output capacitor. Two resonant circuit modules with interleaved PWM scheme are adopted in the proposed converter to reduce the current stress of active and passive components and reduce the ripple current at output side. In each circuit module, one flying capacitor is added between two half-bridge legs to balance two input capacitor voltages. Two resonant converter are connected in series in order to reduce the voltage stress of each MOSFET at \( V_{in}/2 \). The pulse frequency modulation scheme is used to regulate output voltage. The switching frequency is controlled to be less than the series resonant frequency so that MOSFETs can be turned on at ZVS and rectifier diodes can be turned off at ZCS. The switching loss of MOSFETs is reduced and the reverse recovery loss of rectifier diodes is overcome. Finally, experiments based on a laboratory prototype are provided to verify the effectiveness of the proposed converter.

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References

Analysis of an Interleaved Resonant Converter for High Voltage and High Current Applications


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