Investigation of InAs/InGaAs/InP Heterojunction Tunneling Field-Effect Transistors

Hye Rim Eun*, Sung Yun Woo*,†, Hwan Gi Lee*, Young Jun Yoon*, Jae Hwa Seo*, Jung-Hee Lee*, Jungjoon Kim* and In Man Kang*,††

Abstract – Tunneling field-effect transistors (TFETs) are very applicable to low standby-power application by their virtues of low off-current (I_{off}) and small subthreshold swing (S). However, low on-current (I_{on}) of silicon-based TFETs has been pointed out as a drawback. To improve I_{on} of TFET, a gate-all-around (GAA) TFET based on III-V compound semiconductor with InAs/InGaAs/InP multiple-heterojunction structure is proposed and investigated. Its performances have been evaluated with the gallium (Ga) composition (x) for In_{1-x}Ga_xAs in the channel region. According to the simulation results for I_{on}, I_{off}, S, and on/off current ratio (I_{on}/I_{off}), the device adopting In_{0.53}Ga_{0.47}As channel showed the optimum direct-current (DC) performance, as a result of controlling the Ga fraction. By introducing an n-type InGaAs thin layer near the source end, improved DC characteristics and radio-frequency (RF) performances were obtained due to boosted band-to-band (BTB) tunneling efficiency.

Keywords: Gate-all-around, InAs / InGaAs / InP heterojunction, Tunneling field-effect transistor, TCAD

1. Introduction

As the channel length (L_{ch}) of conventional MOSFET scales down continuously, various problems such as short-channel effects (SCEs) and high standby-power dissipation have been witnessed. Recently, tunneling field-effect transistor (TFET) based on band-to-band (BTB) tunneling mechanism has been researched as one of solutions for ultra-small MOSFETs aiming low standby-power applications. Owing to its merits including low off-current (I_{off}) and small subthreshold swing (S), TFETs can be used in low-power and high-speed applications [1-4]. On the other hand, commercializing the silicon-based TFETs has not been successful due to their low on-current (I_{on}) characteristics. To enhance I_{on}, various kinds of compound semiconductors, structures, and gate insulator materials have been adopted to realize advanced TFETs. Especially as using source material of the high mobility and low energy band gap compared with Si, III-V compound semiconductors has been attracted such as InAs and InGaAs for TFETs [5-14].

In this paper, an InAs/InGaAs/InP multiple-heterojunction is applied to gate-all-around (GAA) TFETs. The gallium (Ga) composition (x) in the In_{1-x}Ga_xAs-channel affects the total current, which makes it to be a control variable in optimizing the device performances. Other than searching for an optimum x, n-type doping in the InGaAs channel was introduced to study doping effects. Moreover, radio-frequency (RF) parameters were extracted from devices with different n-type channel lengths (L_{n|InGaAs}).

2. Device characteristics

Fig. 1(a) shows a schematic of the proposed TFET with L_{ch} = 30 nm, channel radius (R_{ch}) = 10 nm, and gate oxide thickness (T_{ox}) = 2 nm. The gate oxide was alumina (Al_{2}O_{3}). The doping concentrations of p+-source, p-channel, and n+-drain regions were 10^{20}, 10^{16}, and 10^{18} cm^{-3}, in sequence.

![Fig. 1. Schematics of the GAA InAs/InGaAs/InP heterojunction TFETs (a) without and (b) with the n' insertion layer near the source junction.](image-url)
Devices were simulated with the trap-assisted tunneling (TAT) and nonlocal band-to-band (BTB) tunneling model showing higher accuracy compared to models with fixed constants provided in the device simulation package [15]. In fabrication, InGaAs and InAs can be epitaxially grown on InP substrate by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) to make up the InAs/InGaAs/InP heterojunctions [16]. The lattice constant of InAs, In0.53Ga0.47As, and InP are 6.058 Å, 5.869 Å, and 5.869 Å, respectively, at room temperature [17]. In analyzing the simulation results, S was defined as the average slope between the onset point of drain current (\(I_D\)) and the reference point at \(I_D = 10^{-7} \text{A/\mu m}\) on the \(I_D-V_{GS}\) transfer curve. \(I_{on}\) was \(I_0\) at \(V_{GS} = V_{DS} = 0.5 \text{V}\) (\(I_D\): drain current, \(V_{GS}\): gate-to-source voltage, \(V_{DS}\): drain-to-source voltage). The device in Fig. 1(b) is equipped with an additional n-type region near the source end to enhance the tunneling.

Fig. 2(a) shows the transfer curves of the proposed TFETs with different \(x\) values in In\(_x\)Ga\(_{1-x}\)As. Tunneling probability, \(T(E)\), induced from Wentzel-Kramers-Brillouin (WKB) approximation is expressed as follows:

\[
T(E) = \exp\left(-\frac{4\sqrt{2m^*E_g^{3/2}}}{3|e|\hbar^2}\right)
\]

where \(m^*\) is the reduced effective mass of \(m = (m_e^*m_h^*)/(m_e^* + m_h^*)\) considering \(m_e^*\) and \(m_h^*\), electron and hole effective masses, \(E_g\) is energy bandgap, \(|e|\) is electron charge, \(\xi\) is the electric field, and \(\hbar\) is the reduced Planck’s constant (\(\hbar/2\pi\)) [18,19]. As the Ga fraction gets lower, \(m^*\) and \(E_g\) become smaller [20]. As shown in Eq. (1), \(T(E)\) increases in terms of smaller \(m^*\) and \(E_g\). For source InAs, \(m^* = 0.0248\) \(m_0\) and \(E_g = 0.35\) eV as listed in the table of Fig. 2(b), by which greatly enhanced \(T(E)\) is expected [20,21]. Due to a relatively larger \(E_g\) of InP (1.34 eV), BTB tunneling between drain and channel in the off-state restrains ambipolar behavior mainly due to gate-induced drain leakage (GIDL). As shown in Fig. 2(b), even though \(E_g\) of channel InGaAs gets larger with higher Ga fraction, the source-to-channel effective tunneling barrier width does not change drastically. From the viewpoint of \(I_{off}\) and ambipolar behavior, higher \(x\) results in thicker channel-to-drain tunneling barrier, which effectively suppresses \(I_{off}\).

Fig. 3 shows the \(I_{on}\), \(I_{off}\), \(S\), and \(I_{on}/I_{off}\) for the simulated devices as a function of \(x\). As shown in Fig. 3(a), it is observed that both \(I_{on}\) and \(I_{off}\) decrease as \(x\) increases. These parameters are in trade-off relation and higher \(I_{on}\) and lower \(I_{off}\) cannot be obtained at the same time. Thus, it

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**Fig. 2.** Transfer characteristics: (a) \(I_D-V_{GS}\) curves of GAA InAs/InGaAs/InP TFETs with different Ga fractions in the channel; (b) Energy-band diagrams along the channel with different Ga fractions at \(V_{GS} = V_{DS} = 0.5 \text{V}\).

**Fig. 3.** Direct-current (DC) characteristics: (a) \(I_{on}\) and \(I_{off}\); (b) \(S\) and \(I_{on}/I_{off}\) as a function of \(x\).
is necessary to put a weight on a narrowed number of parameters of interest in determining the Ga fraction. Fig. 3(b) shows $S$ and $I_{on}/I_{off}$ as a function of $x$. $I_{on}/I_{off}$ at $x = 0.47$ ($2.4 \times 10^8$) is 10 times higher than the value at $x = 0.1$. Also, $S$ at $x = 0.47$ (32.4 mV/dec) is smaller compared with $x = 0.1$ case. $x = 0.47$ (In$_{0.53}$Ga$_{0.47}$As) can be a very good selection from $S$ and $I_{on}/I_{off}$ viewpoint but it might be also changed to a lower value if $I_{on}$ is regarded as the parameter of main interest (Fig. 3(a)).

In reference to InAs homojunction GAA TFET indicated in a previous work [22], the purposed InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFET has been investigated for lower standby power application at drain voltage ($V_{DS}$) of 0.2 V. Due to low $V_{DS}$, the ambipolar behavior of InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFET is more restrained as shown in Fig. 4. Although there are differences in the effective masses according to various channel diameters due to confinement, the electron effective mass of InAs in InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFETs is close to the bulk value of 0.023 $m_0$ as $d = 20$ nm [22]. So, InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFET has high current level.

3. n$^-$-In$_{0.53}$Ga$_{0.47}$As Tunneling-boost layer

Fig. 1(b) showed a schematic of GAA InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFET with very thin n-type layer near the source junction. The locally introduced n-type region improves device performances. The n-type doping concentration was $5 \times 10^{19}$ cm$^{-3}$.

Fig. 5 (a) shows the $I_{D}-V_{GS}$ transfer curve of TFETs having n-type insertion layer with different lengths. Fig. 5 (b) shows $S$ and $I_{on}$ extracted from the transfer curves. In consideration of $S$ and $I_{on}$, $L_{n|InGaAs}$ of 3 nm can be considered to be an optimum value, where $I_{on}/I_{off} = 4.78 \times 10^8$, $S = 21$ mV/dec, and $I_{on} = 1.33$ mA/μm were obtained. The optimum values are more valued than those of GAA InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFETs without n-type layer, where $I_{on}/I_{off} = 2.4 \times 10^8$, $S = 32.4$ mV/dec, and $I_{on} = 368$ μA/μm, respectively.

Fig. 6 shows RF performances in terms of cut-off frequency ($f_T$), maximum oscillation frequency ($f_{max}$), and intrinsic delay time ($\tau$) of InAs/In$_{0.53}$Ga$_{0.47}$As/InP TFETs with (filled circles) and without (open circles) the thin n-type insertion layer (thickness = 3 nm) to boost the tunneling efficiency. $f_T$ and $f_{max}$ are expressed as follows [23]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_g)}$$

(2)

$$f_{max} = \frac{f_T}{\sqrt{4R_{g,s}(g_{ds} + 2\pi f_T C_{gs})}}$$

(3)
where $g_{ds}$, $g_{ss}$, $R_{g,off}$, $R_{on}$, and $R_{g}$ are the transconductance, source-drain conductance, external source resistance, external gate resistance, and gate resistance, in sequence. $C_{gd}$ and $C_{gs}$ are gate-drain and gate-source capacitances, respectively. From Eq. (2), $f_t$ is determined by input capacitance and $g_{m}$. The n-type insertion layer has an effect on $C_{gs}$ and $g_{m}$. In case of a TFET, the inversion charges start to accumulate from drain to source direction with increasing $V_{GSS}$ [24], which makes $C_{gd}$ larger than $C_{gs}$. Since $C_{gd}$ is dominant, the effect of $L_{InGaAs}$ is insignificant on the sum of $C_{gd}$ and $C_{gs}$. $f_t = 2.5$ tera-hertz (THz) and $f_{max} = 3$ THz were obtained from the TFET with n-type tunneling-booster region, which are much higher than those from device without the thin layer. Although the current level of conventional TFETs must be deteriorated by tunneling barrier, the GAA InAs/In0.53Ga0.47As/InP TFET with n-type insertion layer demonstrates good RF performance due to its genuinely high current level. $\tau$ is defined by the following equation [25,26]:

$$\tau = \frac{(C_{gd} + C_{gs})}{g_{m}}$$

From Eq. (4) and the simulation results, $\tau$s were 14.5 femto-seconds (fs) and 20.6 fs for the devices with and without the n-type insertion layer.

4. Conclusion

A GAA InAs/InGaAs/InP heterojunction TFET has been designed and optimized in terms of Ga fraction and its performances were investigated by simulation works. When $x$ for channel In$_{1-x}$Ga$_x$As was selected to be 0.47 as an optimum value, $I_{on} = 368$ mA/µm, $S = 32.4$ mV/dec, and $L_{on}/I_{on}$ ratio = 2.41×10$^6$ were obtained. At the same Ga fraction, n-type thin layer with an optimum thickness of 3 nm was schemed for improvements in the RF performances as well as DC characteristics ($I_{on}$ of 1.33 mA/µm and S of 21 mV/dec). Both $f_t$ and $f_{max}$ in the THz-regime were traced from the optimized TFET device. It supports that optimally designed InAs/InGaAs/InP heterojunction TFET has a strong potential for high-performance DC and RF applications.

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Hye Rim Eun She received the B.S. degree in physics engineering from the Department of Physics, Andong National University (ANU), Andong, Korea, in 2014. She is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). Her research interests include design, fabrication, and characterization of compound CMOS, tunneling FET, and GaN-based devices.

Sung Yun Woo He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2014. He is currently working toward the M.S. degree in electrical engineering with School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU). His research interests include design, fabrication, and characterization of NAND flash memory, silicon-based 3D devices, and neuromorphic technology devices.

Hwan Gi Lee He received the B.S. degree in physics education from the Department of Physics Education, Daegu University, Daegu, Korea, in 2011. He is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of nanoscale CMOS, LED, and GaN-based devices.

Young Jun Yoon He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2013. He is currently working toward the M.S. degree in electrical engineering with the School
Hye Rim Eun, Sung Yun Woo, Hwan Gi Lee, Young Jun Yoon, Jae Hwa Seo, Jung-Hee Lee, Jungjoon Kim and In Man Kang

of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of nanoscale tunneling FET, GaN-based transistors, and GaN-based circuit.

Jae Hwa Seo He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2012. He is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of nanoscale CMOS, tunneling FET, III-V compound transistors, and junctionless silicon devices.

Jung-Hee Lee He received the B.S. and M.S. degrees in electronic engineering from Kyungpook National University, Daegu, in 1979 and 1983, respectively, the M.S. degree in electrical and computer engineering from Florida Institute of Technology, Melbourne, in 1986, and the Ph.D. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 1990. His doctoral research concerned carrier collection and laser properties in monolayer-thick quantum-well heterostructures. From 1990 to 1993, he was with the Compound Semiconductor Research Group, Electronics and Telecommunication Research Institute, Daejeon, Korea. Since 1993, he has been a Professor with the School of Electronics Engineering (SEE), Kyungpook National University, Daegu. He is the author or coauthor of more than 200 publications on semiconductor materials and devices. His current research is focused on the growth of nitride-based epitaxy, the fabrication and characterization of gallium-nitride-based electronic and optoelectronic devices, atomic layer epitaxy for metal-oxide-semiconductor application, and characterizations and analyses for the 3-D devices such as fin-shaped FETs.

Jungjoon Kim He received his B.S. degree in electronic engineering from Kyungpook National University, Daegu, Korea and his M.S. degree in electronic engineering from KAIST, Daejeon, Korea. He received his Ph.D. degree in electrical and computer engineering from Louisiana State University, U.S. He has been a Profesor with the School of Electrical Engineering and Computer Science, Kyungpook National University, since 2012.

In Man Kang He received the B.S. degree in electronic and electrical engineering from School of Electronics and Electrical Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2001, and the Ph.D. degree in electrical engineering from School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU), Seoul, Korea, in 2007. He worked as a teaching assistant for semiconductor process education from 2001 to 2006 at Inter-university Semiconductor Research Center (ISRC) in SNU. From 2007 to 2010, he worked as a senior engineer at Design Technology Team of Samsung Electronics Company. In 2010, he joined KNU as a full-time lecturer of the School of Electronics Engineering (SEE). Now, he has worked as an assistant professor. His current research interests include CMOS RF modeling, silicon nanowire devices, tunneling transistor, low-power nano CMOS, and III-V compound semiconductors. He is a member of IEEE EDS.